L Number	Hits	Search Text	DB	Time stamp
1	1	6265902.pn. and reset	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 13:45
-	27	pll and reset and (slip adj1 detect$3)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 11:06
-	3	("6037806" | "6133769" | "6404240").PN.	USPAT	2003/09/24 13:41
-	4	("4030045" | "4620300" | "4733197" | "5790613").PN.	USPAT	2003/09/24 13:44
-	5	("3723889" | "4901026" | "4902920" | "5164838" | "5790613").PN.	USPAT	2003/09/24 13:50
-	402	pll and reset and (slip$4)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 11:06
-	235	(pll and reset and (slip$4)) and flip-flop$1	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 11:08
-	210	((pll and reset and (slip$4)) and flip-flop$1) and delay$3	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 11:08
-	200	(((pll and reset and (slip$4)) and flip-flop$1) and delay$3) and divid$3	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 13:45
-	5	((((pll and reset and (slip$4)) and flip-flop$1) and delay$3) and divid$3) and (up near3 slip$)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 11:10
-	19	((((pll and reset and (slip$4)) and flip-flop$1) and delay$3) and divid$3) and (up with slip$)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 11:10
-	4	("4030045" | "4620300" | "4733197" | "5790613").PN.	USPAT	2004/06/25 11:13
-	5	("3723889" | "4901026" | "4902920" | "5164838" | "5790613").PN.	USPAT	2004/06/25 11:44

United States Patent [19]

Oberst

[11] **3,723,889**

[45] **Mar. 27, 1973**

[54] **PHASE AND FREQUENCY COMPARATOR**

[75] Inventor: **James Francis Oberst, Howell Twp., Monmouth County, N.J.**

[73] Assignee: **Bell Telephone Laboratories, Incorporated, Murray Hill, N.J.**

[22] Filed: **Dec. 22, 1971**

[21] Appl. No.: **210,644**

[52] U.S. Cl. **328/134, 328/94, 328/99, 307/233, 307/218, 307/217, 307/225, 328/110**

[51] Int. Cl. **H03d 13/00**

[58] Field of Search......307/233, 232, 228, 225, 218, 307/217; 328/133, 134, 94, 99, 110

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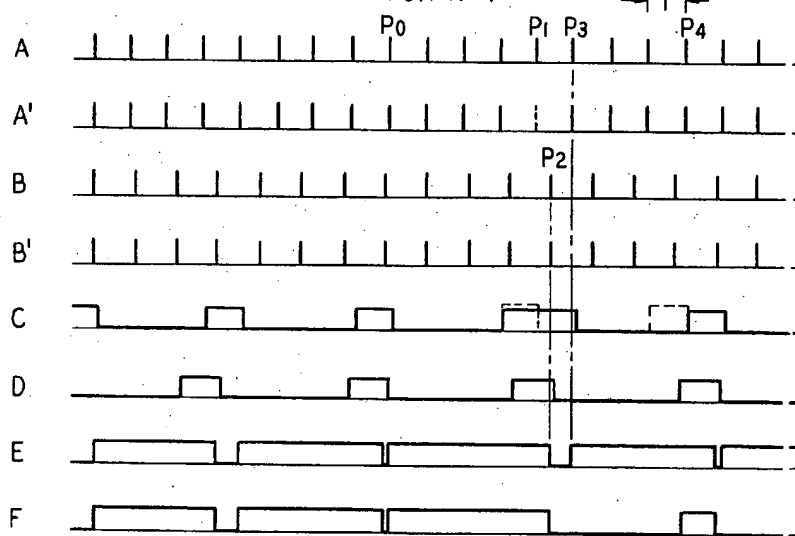|			
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[57] **ABSTRACT**

A sawtooth phase comparator is arranged to act as a frequency comparator when the frequencies of the input and reference signals differ by a substantial amount. This is accomplished by using a phase comparator consisting of a flip-flop with first and second frequency counters connected between the input signal and its SET input, and between the reference signal and its RESET input, respectively. Means are provided for inhibiting the input signal whenever it would cause a signal to appear at the set input of the flip-flop when it is already set and for inhibiting the reference signal whenever it would cause a signal to appear at the RESET input when it is already reset. This eliminates the alternating polarity signal which prior art comparators produce when the linear portion of the transfer characteristic is exceeded. Consequently, a frequency correcting signal is produced.

5 Claims, 3 Drawing Figures

FIG. 1

FIG. 2
FOR N=4

FIG. 3

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PHASE AND FREQUENCY COMPARATOR

BACKGROUND OF THE INVENTION

This invention relates to phase-locked loops and, more particularly, to combination phase and frequency comparators (PFC), which are useful in phase-locked loops.

In a basic phase-locked loop an input signal and a reference signal from a local voltage-controlled oscillator (VCO) are compared in a phase detector. The output of the phase detector, representing the difference in phase between the two signals, is then used to vary the output of the VCO in such a way that it is made equal in phase to the input signal. One of the most basic types of phase comparators consists of an R-S (Reset-Set) flip-flop with the input signal applied to its SET input and the reference signal applied to the RESET input. With this arrangement the width of the output pulse of the flip-flop will indicate the phase difference between the two signals. The pulsed output is then integrated in a low-pass filter to generate a dc signal which is used to control the output of the VCO.

The transfer function of this phase comparator resembles a sawtooth pattern which repeats every 360°. This can be seen from the fact that the comparator output is nearly zero when the two signals have about the same phase relationship. As the phase difference increases, the pulse width increases, causing a corresponding increase in the output of the filter. This generates the ramp portion of the sawtooth characteristic. However, if the input signal had been leading the reference signal and the phase error increases to the point where a reference pulse occurs before the input pulse, the circuit will change states and the pulse width will become small again. This occurs because the reference pulse has slipped a cycle and is now almost in phase coincidence with the succeeding input pulse. This change of states causes the output of the filter to drop abruptly to zero, thus completing the sawtooth characteristic. In this type of circuit a dc bias voltage is usually applied to the filter so that the characteristic will be symmetrical about zero.

When the frequencies of the input and test signals differ by a significant amount, the circuit will continually slip cycles and will produce a signal which alternates between positive and negative values. When this alternating signal is applied to the VCO of the phase-locked loop, the loop will not be able to acquire a lock since it will not know whether the positive or the negative signal is the correct one. This problem is partially solved by putting digital counters or frequency dividers between the input signal and the SET input, and between the reference signal and the RESET input of the flip-flop, respectively. This extends the ramp portion of the sawtooth characteristic from ±180 degrees to ±(N × 180) degrees, where N is the division achieved by the divider circuit. Therefore, the acquisition range has been increased by a factor of N. However, if this expanded range is exceeded, the alternating signal will still occur. This will usually happen when the frequencies of the input and reference signals differ by a substantial amount. In order to correct this situation, a frequency detector must be used to produce a signal which will control the VCO in such a way that the two frequencies will be matched. Then the phase detector will take over and cause the VCO output to match the phase of the input signal.

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It is therefore an object of this invention to provide a circuit which will modify the operation of the the simple flip-flop phase detector so that it will function as a combination phase and frequency detector.

SUMMARY OF THE INVENTION

The present invention is directed to expanding the acquisition range of a simple one flip-flop phase detector with counters by modifying its operation to include frequency detection. This is accomplished by inhibiting the SET or RESET inputs when the flip-flop is already set or reset, respectively. This invention is particularly useful since with the addition of a relatively small number of parts it allows for an improvement in the many systems which utilize the one flip-flop phase detector with counters.

In an illustrative embodiment of the invention, counter circuits allow one of every N pulses of the input and reference signals to be applied to the SET and RESET inputs of a flip-flop, respectively. The state of the flip-flop and the counters is then monitored in first and second AND gates. When it appears that the counter is in a condition which will allow an input pulse to reach the SET input when the flip-flop is already set, the first AND gate will cause the input pulse to be blocked, thus giving the reference pulse an opportunity to reset the flip-flop before the next input pulse occurs. The second AND gate performs the same function for the RESET line. This prevents the average output level from making a dramatic change. Therefore, when the output is passed through a low-pass filter and is biased about zero, it will remain positive when the input frequency is higher than the reference frequency and negative when it is lower. This, in effect, makes the circuit operate as a frequency detector when the frequencies are not matched and a phase detector when they are.

The foregoing and other features of the present invention will be more readily apparent from the following detailed description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic of an illustrative embodiment of the invention;

FIG. 2 is a timing diagram for the circuit of FIG. 1; and

FIG. 3 is a transfer characteristic for the circuit of FIG. 1.

DETAILED DESCRIPTION

FIG. 1 is a schematic of a single flip-flop phase detector, modified to act as a phase and frequency comparator (PFC) according to the principles of the present invention. In FIG. 1 the input signal, V_1, represented by curve A in FIG. 2, is applied to the normal input of INHIBIT gate 10. The reference or VCO signal, V_2, represented by curve B in FIG. 2, is applied to the normal input of INHIBIT gate 11. Then the output of INHIBIT gate 10 is applied both to the input of counter circuit 12 and to the first input of two-input AND gate 14. In a similar manner, the output of INHIBIT gate 11 is applied to the input of counter circuit 13 and to the first input of two-input AND gate 15. These output signals from the INHIBIT gates are shown as curves A' and B' in FIG. 2. The counter circuits (12 and 13)

allow one of N pulses of the outputs of the INHIBIT gates to pass through them. For the purpose of this embodiment N is assumed to equal 4. The outputs of the counter circuits 12 and 13, represented by solid curves C and D in FIG. 2, are applied to the second inputs of two-input AND gates 14 and 15, respectively. In addition, the output of counter 12 is applied to the first input of two-input AND gate 16 and the output of counter 13 is applied to the first input of two-input AND gate 17. The output of AND gate 14 is applied to the SET input of flip-flop 18 and the output of AND gate 15 is applied to the RESET input. The Q output of flip-flop 18 which is the circuit output, V_3, is applied to the second input of AND gate 16 and the $\overline{Q}$ output is applied to the second input of AND gate 17. The Q output of the flip-flop is the output which has a digital "1" level when the SET input is triggered and the $\overline{Q}$ output is the one which has a digital "1" level when the RESET input is triggered. The outputs of AND gates 16 and 17 are applied to the inhibit inputs of INHIBIT gates 10 and 11, respectively.

With this arrangement the input and reference signals initially pass through INHIBIT gates 10 and 11 since the outputs of AND gates 16 and 17 will be logical "0's". After passing through the INHIBIT gates, these pulses are then blocked by AND gates 14 and 15 because of the "0" outputs from counter circuits 12 and 13. However, eventually the counter circuits will change states in response to the pulses applied to their inputs. This will then allow a pulse from the output of the INHIBIT gates to reach the flip-flop causing it to change states. In order to accomplish this according to the timing diagram in FIG. 2, the counter outputs must be delayed slightly relative to the pulses at A'. If such a delay does not occur naturally in the counter circuitry, it may be added at the counter input or output.

The phase difference between the two signals is represented by the pulse width of the signals at the Q or $\overline{Q}$ output of the flip-flop. In this case the output is taken from the Q output and it is shown by curve E in FIG. 2. If this circuit were included in a phase-locked loop, this signal would be passed through a low-pass filter to obtain a dc control signal and then biased about zero volts so that there would be a positive signal for a leading phase error and a negative signal for a lagging phase error. The effect of the counter circuits is to extend the linear range of the phase detector from ±180° to N times ±180 degrees. This is shown in the transfer function of FIG. 3 where the linear range for N = 4 extends from −4π to +4π.

If the INHIBIT gates and AND gates 16 and 17 were not part of the circuit, the Q output of the flip-flop would be like curve F in FIG. 2. Since the input frequency is higher than the reference frequency, the output of counter 12 would be at a higher frequency than the output of counter 13. Therefore, it would be possible for the flip-flop to receive two pulses from AND gate 14 before it receives one pulse from AND gate 15. In the timing diagram of FIG. 2, this hypothetical situation is initiated with pulse P_0 of curve A. The dotted curve C shows the output of counter 12 when the INHIBIT gates are not part of the circuit. The first dotted pulse allows the pulse P_1 to reach the SET input of the flip-flop before pulse P_2. Since the flip-flop was already set the pulse P_1 will have no effect. However,

when pulse P_2 arrives at the flip-flop it will cause the flip-flop to reset and remain that way until pulse P_4 is allowed to pass by the second dotted pulse in curve C. As shown by curve F, this causes a drastic change in the average value of the output signal. Since this signal is later integrated and biased about zero, the resulting dc control signal will change from a relatively large positive value to a relatively large negative value. This change is indicated by the path 31 in FIG. 3. The result of this situation is that, even though there has been no change in the frequencies of the input and reference signal, the dc control signal changes polarity and produces an incorrect signal for the VCO. In general, the circuit will continue to slip along its characteristic curve in this manner, generating an alternating polarity signal which prevents the control loop from locking.

When the INHIBIT gates (10 and 11) and AND gates (16 and 17) are included in the circuit, the Q output is like that shown in curve E of FIG. 2. In this case, AND gate 16 monitors the output of counter 12 and the Q output of the flip-flop. When the pulse P_1 attempts to get through to the SET input of the flip-flop, AND gate 16 causes INHIBIT gate 10 to block it, since the counter and the Q outputs are both at logical "1's." This also prevents the pulse P_1 from reaching the counter circuit causing it to remain high for an additional period as shown by the solid curve C in FIG. 2. Then pulse P_2 passes to the RESET input and the flip-flop is reset. This causes AND gate 16 to remove the blocking signal from INHIBIT gate 10 and allows pulse P_3 to set the flip-flop at the next timing period.

The result of this is that there is only a small change in the average value of the output signal when the linear portion of the transfer characteristic is exceeded. Although an alternating signal is produced, it is not great enough to change the polarity of the dc control signal for the VCO. This is represented by path 30 in FIG. 3. Since the signal remains positive, the VCO will continue to increase its frequency until it matches the input signal. Then the circuit will operate on one of the linear segments of the transfer curve, and phase matching will occur. It should be noted that if the input signal were lower in frequency than the reference signal, the circuit would function in the same manner except that INHIBIT gate 11 would be blocking additional RESET pulses and the circuit would operate along curve 32 in FIG. 3. In addition, it should be noted that the amount of ripple shown by FIG. 3 is directly proportional to the frequency division in the counter circuits. Therefore, by increasing the value of N, the amount of ripple in the dc control signal for the VCO can be reduced.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

We claim:

1. A phase and frequency comparator which compares the phase and frequency of an input signal with that of a reference signal and produces an output signal related to the difference in phase and frequency, comprising:

means for inhibiting the input and reference signals in response to first and second inhibit signals;

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means for separately counting the pulses of the input and reference signals which pass through said means for inhibiting and for producing output levels for every Nth pulse;

switching means, responsive to the outputs of said means for inhibiting and said means for separately counting, for producing first and second complementary digital signals, the first complementary signal being the output of said comparator; and

means for generating the first and second inhibit signals in response to the output of said means for separately counting, and said switching means.

2. A comparator as claimed in claim 1 wherein said means for inhibiting comprises:

a first INHIBIT gate with the input signal applied to the normal input and the first inhibit signal applied to the inhibit input; and a second INHIBIT gate with the reference signal applied to the normal input and the second inhibit signal applied to the inhibit input, the outputs of said first and second INHIBIT gates being said pulses which pass through said means for inhibiting.

3. A comparator as claimed in claim 2 wherein said means for separately counting comprises:

a first counter circuit for producing an output level for every Nth pulse from said first INHIBIT gate; and

a second counter circuit for producing an output level for every Nth pulse from said second IN-HIBIT gate.

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4. A comparator as claimed in claim 3 wherein said switching means comprises:

a first AND gate for combining the outputs of said first counter circuit and said first INHIBIT gate;

a second AND gate for combining the outputs of said second counter circuit and said second INHIBIT gate; and

a reset-set flip-flop having complementary Q and $\overline{Q}$ outputs, the Q output being at a high digital level when the SET input is activated and the $\overline{Q}$ output being at a high digital level when the RESET input is activated, the output of said first AND gate being applied to the SET input of said flip-flop, the output of said second AND gate applied to the RESET input of said flip-flop, the output of the comparator and the first complementary signal being the signal at the Q output of said flip-flop and the second complementary signal being the signal at the $\overline{Q}$ output of said flip-flop.

5. A comparator as claimed in claim 4 wherein said means for generating the first and second inhibit signals comprises:

a third AND gate for combining the Q output of said flip-flop and the output of said first counter circuit, and a fourth AND gate for combining the $\overline{Q}$ output of said flip-flop and the output of said second counter circuit, the output of said third AND gate being the first inhibit signal and the output of said fourth AND gate being the second inhibit signal.

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United States Patent [19]

Phillips et al.

[11] **Patent Number:** **4,901,026**

[45] **Date of Patent:** Feb. 13, 1990

[54] **PHASE DETECTOR CIRCUIT HAVING LATCHED OUTPUT CHARACTERISTIC**

[75] Inventors: **Donald E. Phillips**, Cedar Rapids; **Gregory A. Jobe**, Marion, both of Iowa

[73] Assignee: **Rockwell International Corporation**, El Segundo, Calif.

[21] Appl. No.: 275,803

[22] Filed: **Nov. 23, 1988**

Related U.S. Application Data

[62] Division of Ser. No. 68,877, Jul. 1, 1987, Pat. No. 4,801,896.

[51] Int. Cl.⁴ H03L 7/08; H03K 9/08
[52] U.S. Cl. 328/133; 328/110; 331/25; 307/514
[58] Field of Search .... 328/133, 134, 109, 110, 328/155; 307/514, 516; 331/1 R, 1 A, 25

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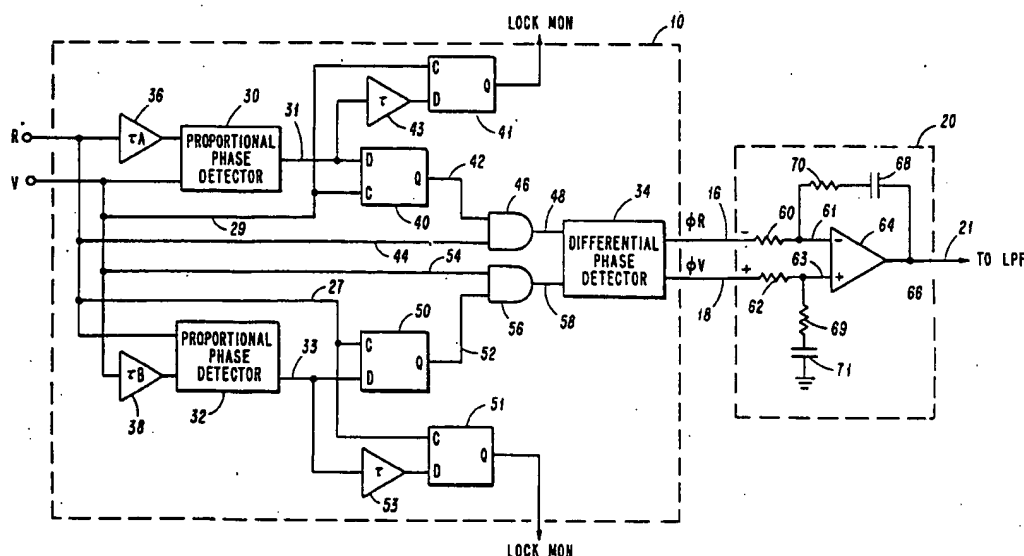
Primary Examiner—Stanley D. Miller
Assistant Examiner—Timothy P. Callahan
Attorney, Agent, or Firm—M. Lee Murrah; V. Lawrence Sewell; H. Fredrick Hamann

[57] **ABSTRACT**

A phase detector circuit for providing an output indicative of the phase relationship between two input signals. The output of the phase detector responds rapidly to changes in the phase relationship between the input signals and avoids "cycling" when this phase relationship is less than -2π or greater than 2π. The phase detector includes circuit means for detecting when the phase relationship is outside a desired range such as proportional phase detectors which operate in combination with a differential type phase detector for providing the required output.
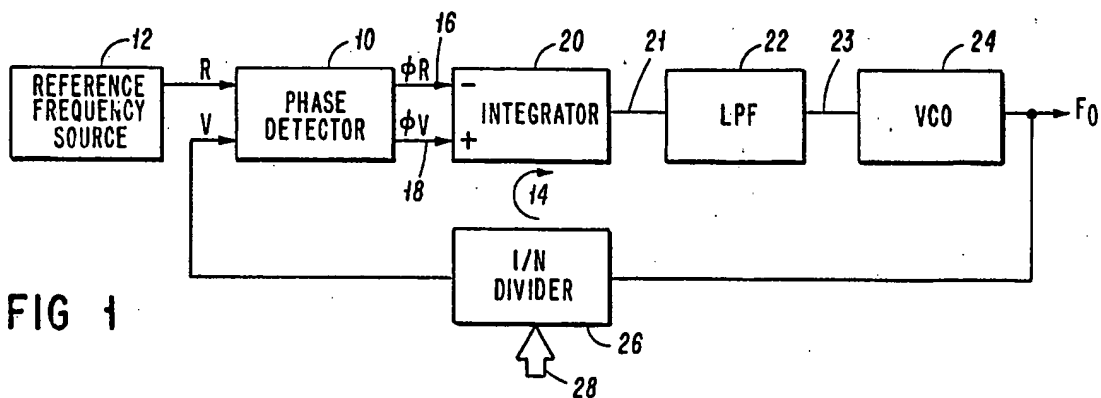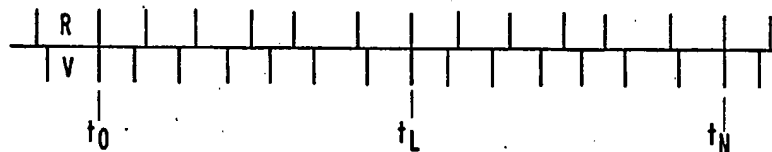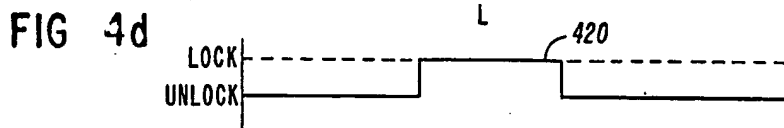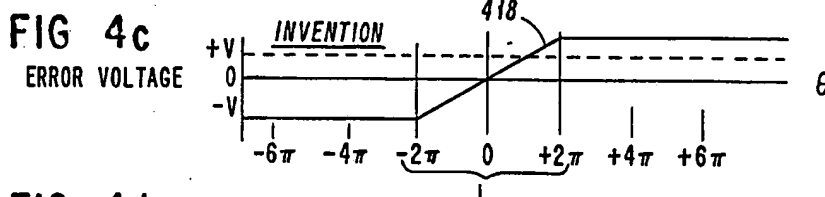
7 Claims, 2 Drawing Sheets

FIG 1

FIG 3a

FIG 3b

FIG 3c

FIG 4a
ERROR VOLTAGE
PRIOR ART

FIG 4b

FIG 4c
ERROR VOLTAGE
INVENTION

FIG 4d

FIG 5

FIG 2

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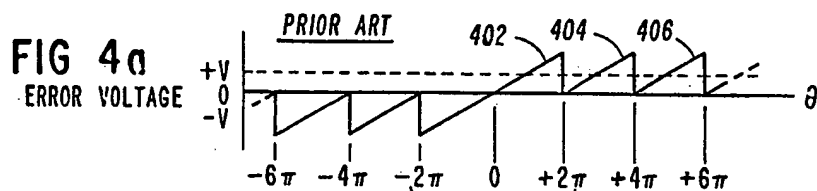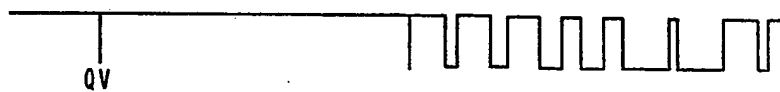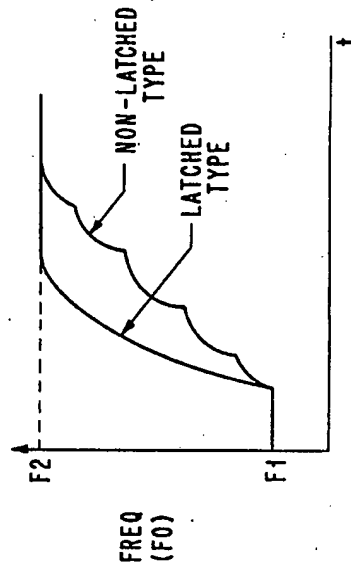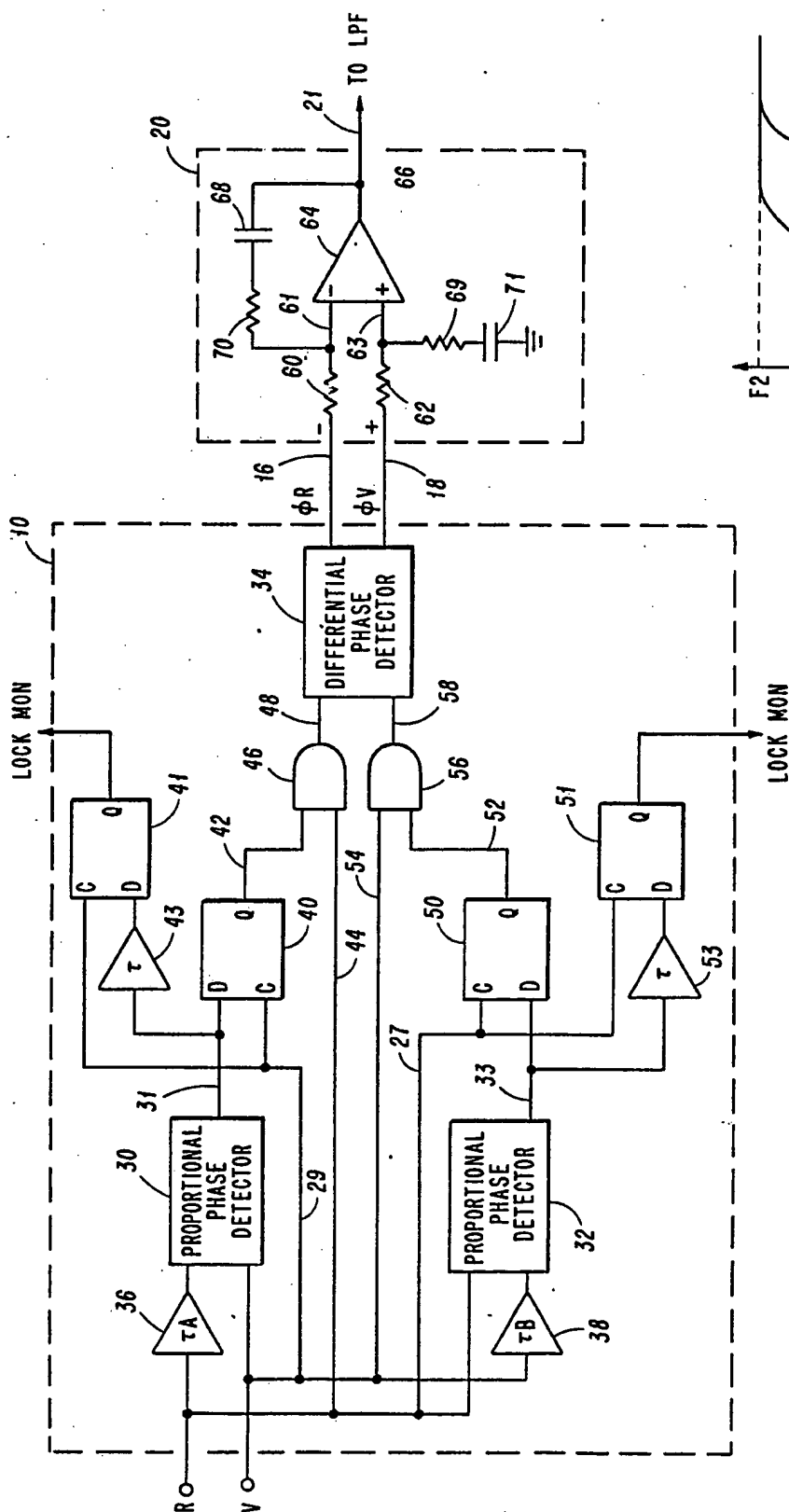# PHASE DETECTOR CIRCUIT HAVING LATCHED OUTPUT CHARACTERISTIC

This application is a divisional of application Ser. No. 068,877 filed on July 1, 1987, now U.S. Pat. No. 4,801,896.

BACKGROUND OF THE INVENTION

The invention relates to radio frequency tuners, and more particularly to such tuners which employ phase-locked-loops as frequency generation elements, and most particularly to phase detectors used in such phase-locked loop radio frequency tuners.

Phase-locked-loops are commonly used in circuits to produce a precise, stable frequency. They can be used both as an oscillator in a receiver to detect signals of prescribed frequency and as a frequency synthesizer in a transmitter to generate an output signal having a selectively variable frequency. The basic elements of a phase-locked-loop (PLL) include a voltage controlled oscillator (VCO) for producing an output signal having a controlled frequency, a detector for comparing the phase of the output signal with that of a predetermined reference signal and for producing an error signal representing the detected phase difference, and a loop filter for filtering the error signal and coupling it to the VCO to controllably adjust the output signal's frequency.

A common use of PLL frequency synthesizers is in frequency hopping radio communications systems which are used for secure communications. These systems use radio transmitters and receivers which hop in synchronization from one frequency to another in a predetermined sequence, transmitting and receiving a small part of a message on each frequency. The security of the frequency hopping technique depends both upon the choice of frequencies and upon the hopping rate. Increasing the hopping rate increases the difficulty of unauthorized monitoring stations in determining the hopping patterns and following the hopping sequence.

The frequency hopping rate is limited primarily by the time required for PLL's to change from one frequency to another. The frequency change rate is affected by a number of factors. For example, the bandwidth of the PLL loop filter significantly limits the frequency change rate. More relevant to the present invention, however, are the limitations due to the phase detector.

Prior art phase detectors of the differential type are subject to "cycling" outside the desired phase lock range as the phase relationship between the reference signal and the VCO output signal changes. This results in an error signal which varies with phase angle, and over several 2π phase ranges exhibits a triangular, "sawtooth" waveform. It is the average level of this signal which is used to urge the VCO toward the desired lock-in range. With the triangular waveforms of prior art detectors, this voltage, and the resulting slew rate, is only 50 per cent of theoretical due to cycling. The VCO output frequency thus changes more slowly than if the peak signal level were used.

Prior art phase detectors are also subject to an ambiguity since it is not possible to determine from the cycling phase detector error signal whether the PLL is within or without the desired lock-in range and thus a momentary false lock-in indication is given. Consequently, there is no positive indication of lock-in, and a

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transmitter cannot be limited to operation only while positively locked onto the selected frequency.

It is therefore an object of the present invention to provide an improved PLL.

It is another object of the present invention to provide a PLL which locks onto the desired frequency more quickly.

It is a further object of the present invention to provide a PLL which permits operation of a radio transmitter only when the PLL is locked onto the desired frequency.

It is an additional object of the present invention to provide a PLL which provides a smoother change from one frequency to another.

It is still another object of the present invention to provide an improved phase detector for use in PLL's.

It is still a further object of the present invention to provide a phase detector which provides a higher level error signal for control of a VCO, outside the desired lock-in range.

It is an additional object of the present invention to provide a phase detector which provides a positive lock-in indication.

SUMMARY OF THE INVENTION

With these and other objects in view, a phase detector circuit operative in response to first and second input signals includes means to generate a signal indicative of the phase relationship between the first and second input signals and means for decoupling first and second input signals from the generating means when a detecting means identifies a phase relationship between the first and second signals which is outside a predetermined range.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be more fully understood by reading the following description of a preferred embodiment thereof in conjunction with the appended drawings, wherein:

FIG. 1 is a block diagram of a phase locked loop circuit employing the present invention.,

FIG. 2 is a block diagram of a phase detector in accordance with the present invention;

FIG. 3 (a,b,c) is a series of timing diagrams illustrating aspects of the operation of the phase detector of FIG. 2;

FIG. 4 (a,b,c,d) is a series of graphs comparing the error voltage produced by phase detectors of the prior art and by that of the present invention as a function of phase angle θ; and

FIG. 5 is a graph comparing the frequency change of the latched phase detector of the present invention to the non-latched phase detectors of the prior art.

DESCRIPTION OF A PREFERRED EMBODIMENT

Referring to FIG. 1, a phase locked loop (PLL) circuit in which the present invention may be used is shown. The phase detector 10 of the present invention is fed a clock signal R from a reference frequency source 12 and a variable signal V from feedback loop 14. Phase detector 10 provides differential output signals Q_R at line 16 and Q_V at line 18, the state of Q_R and Q_V being representative of the phase difference between signals R and V. The difference between Q_R and Q_V is integrated by integrator 20 to produce a DC signal representative of the phase difference between signals R and V.

The integrator output is passed through a low pass filter 22 to remove high frequency components, and the resultant voltage is fed to a voltage controlled oscillator 24 which produces an output signal F_O.

A portion of signal F_O is fed back to a 1/N divider 26 which in conjunction with an input device represented by arrow 28 comprises a tuning apparatus. The output from divider 26 is fed to phase detector 10 as signal V. L Thus, as the divide ratio of 1/N divider 26 is changed by input device 28, phase detector 10 and integrator 20 together produce an error voltage at the input 23 of VCO 24 which is representative of the phase difference between reference signal R and variable signal V. The error voltage changes the output frequency of VCO 24, and this process continues until signals R and V are in phase and the PLL is thus "locked in." When the loop is tuned to a new frequency by input device 28, and the divider ratio of divider 26 is changed, signals R ∂ V are forced out of phase, and the VCO frequency is again changed until a new locked condition is attained.

Referring now to FIG. 2, a block diagram of phase detector 10 and integrator 20 of FIG. 1 are shown. Essentially, phase detector 10 comprises 2π proportional phase, or "type-1", detectors 30 and 32 which slave a differential, or "type-2", phase detector 34 as hereinafter described. Proportional phase detectors 30 and 32 are well known in the art, and their detailed construction and operation will not be repeated here. A description of this type of phase detector is found in U.S. Pat. Nos. 3,431,509 to Andrea and 4,500,852 to Phillips, which are incorporated herein by reference. Likewise, differential phase detector 34 is well-known in the art and is described in application notes for phase frequency detector devices MC4344 and MC4044 by Motorola Semiconductor Products, Inc., Box 20912, Phoenix, AZ. 85036, which is incorporated herein by reference.

Normally differential phase detector 34 operates as illustrated in FIG. 3. Referring to FIG. 3(a), a series of pulses representing reference signal R and variable signal V are shown having a time varying phase relationship. Pulses V are shown as negative-going while pulses R are shown as positive-going, but it should be understood that the relative polarities are unimportant and may be taken into account using well-known standard circuit design techniques. Further, although signals R and V may actually be square waves in their original form, the use of edge-triggered devices in the circuitry effectively convert them to the pulse form as illustrated. It should be noted that the pulse spacing of signal R is not equal to the pulse spacing of signal V, to represent a frequency difference. Immediately after time t_O, the V pulses lead the R pulses by increasing amounts, until the phase difference disappears and they are in phase at time t_L, and again at time t_N after another whole cycle has slipped.

The outputs Q_R and Q_V of differential phase detector 10 are shown

in FIG. 3(b) and 3(c), respectively. Waveforms Q_R and Q_V comprise a series of rectangular waveforms whose width is proportional to the phase difference between signals R and V. As is characteristic of this type of phase detector, the Q_R output provides a signal when the R pulse is leading the V pulse, and the Q_V output provides a signal when the V pulse is leading the R pulse.

If the pulse streams R and V in FIG. 3(a) were to be continued prior to t_O, the Q_R output pattern would be

repeated the same as between t_O and t_L. Similarly, if the pulse streams R and V were to be continued after t_N, the Q_V output pattern would be repeated the same as between t_L and t_N.

When signals Q_R and Q_V are integrated by integrator 20 and filtered by LPF 22, the average voltage at point 23 varies as shown in FIG. 4(a) as the phase of R and V is varied over several complete cycles. Note that the integrator generates the integral of the difference between Q_R and Q_V as indicated by the polarity symbols at the input of integrator 20. Note that the waveform repeats itself before -2π and after $+\pi$. Thus, the differential phase detector does not provide a stable lock indicator signal within the range L which is defined as $-2\pi < \theta < 2\theta$. If the output voltage is a level $+V_1$, for example, it is not possible to know whether the phase relationship is a point 402, 404, or 406, for example. Thus, for any voltage level it is impossible to determine whether the PLL is in the lock range L or whether it is outside the range L and is merely "cycling." The ambiguity reflects itself in the lock monitor signal shown in FIG. 4(b). In addition to the correct lock signal at 408, erroneous lock monitor signals are also provided at 410, 412, 414, and 416.

Returning now to FIG. 2 the purpose of proportional phase detectors 30 and 32 is to detect when the phase relationship between signals R and V is outside the 4π lock range L [see FIG. 4(a)] and to prevent R and V pulses from entering differential phase detector 34 if that phase relationship exists. In effect differential phase detector 34 is slaved to proportional phase detectors 30 and 32. More particularly, reference signal R and variable signal V as previously described are both simultaneously fed to proportional phase detectors 30 and 32. Signal R is delayed in the input to phase detector 30 by an amount A by delay device 36, and signal V is similarly delayed in the input to phase detector 32 by an amount B by delay device 36. Delay devices 36 and 38 delay signals R and V to compensate for propagation delays in the various components comprising phase detector 10.

Phase detector 30 operates by searching for two V pulses in a row before receiving an R pulse. This condition indicates that the phase relationship has exceeded the 2π range for that detector. When this condition occurs, the "D" input of a flip flop 40 will be in a low state during its clock "C" (from input V), which lowers the logic level on line 42 and prevents the R pulse on line 44 from passing through AND-gate 46 to differential phase detector 34 via line 48. A return to the locked state occurs when there are two R pulses in a row before a V pulse, which causes the "D" input 31 to return to a high state during the clock V, thereby allowing the differential phase detector 34 to be clocked by R. Thus, proportional phase detector 30 and the described associated components prevent passage of R pulses to differential phase detector 48 if the phase relationship is outside the 2π range of detector 30.

The other one-half of the 4π lock range L is controlled by a similar circuit comprised of proportional phase detector 32, a flip flop 50, and an AND-gate 56. Thus if two R pulses in a row are detected before a V pulse, flip flop 50 is toggled lowering the logic level on line 52, thereby preventing the passage of V pulses from line 54 through AND-gate 56 to differential phase detector 34 via line 58. Two V pulses in a row will be detected by the proportional phase detector 32, causing

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flip-flop 50 to toggle to a high level, allowing V pulses to again clock the differential phase detector 34.

Lock monitor signals are provided by flip-flops 41 and 51. Flip-flop 41 has its "C" input coupled to the V signal on line 29 and its output to line 31 through a delay device 43. Similarly, flip-flop 51 is coupled at its "C" input to signal V on line 27 and at its "D" input to line 33 through a delay device 53.

The Q_R and Q_V outputs from differential phase detector 34 are coupled to the inverting (−) and non-inverting (+) inputs 16 and 18, respectively, of integrator 20. Integrator 20 is of conventional design, having resistors 60 and 62 coupled to the inverting and non-inverting inputs 61 and 63, respectively, of a differential operational amplifier 64. Op amp 64 has a feedback path from its output 66 through a capacitor 68 and a resistor 70 to inverting input 61, and a corresponding resistor 69 and capacitor 71 from the non-inverting input 63 to ground. The output 66 of op amp 64 is coupled to low pass filter 22 (FIG. 1) in line 21.

The resulting waveform at line 21 is shown in FIG. 4(c). Below −2π the output voltage on lines 21 and 23 (FIG. 1) for controlling VCO 24 is a constant −V_1, while above 2π the control voltage is a constant +V. Thus, for any voltage +V, an unambiguous phase relationship 418 is provided and a positive lock-in indication is given. In addition, lock-in speed, or slew rate, is increased since the average voltage below −2π and above 2π is greater for the waveform of FIG. 4(c) than for that of FIG. 4(a). Specifically, the average voltage of the repetitive triangular waves of FIG. 4(a) is only one-half that of the constant voltage level of FIG. 4(c). This faster tune characteristic is illustrated in FIG. 5 in that the latched type detector of the present invention provides a more steeply sloped frequency change rate than the non-latched type phase detector of the prior art. Further, the application of the stable voltage from the latched type phase detector of the present invention provides a smoothly varying output frequency F_o as VCO 24 changes from frequency F_1 and seeks a new lock condition at frequency F_2, as illustrated in FIG. 5. By contrast the sawtooth lock in voltage provided to the VCO by the non-latched phase detector of the prior art produces a varying and abruptly changing rate of frequency change as the VCO changes from F_1 to F_2, as also illustrated in FIG. 5.

The lock monitor signal corresponding to the error signal waveform of FIG. 4(c) is shown in FIG. 4(d). A positive lock signal 420 corresponding to the 4π range of the detector is provided by flip-flops 41 and 51, in comparison to the signal of FIG. 4(b) which is cluttered with false indications.

While particular embodiments of the present invention have been shown and described, it is obvious that minor changes and modifications may be made therein without departing from the true scope and spirit of the invention. It is the intention in the appended claims to cover all such changes and modification.

We claim:

1. A phase detector circuit operative in response to first and second input signals having a phase relationship, comprising:

means for generating a signal indicative of said phase relationship between the first and second input signals; means for detecting when said phase relationship between the first and second input signals is outside a predetermined desired range; and means responsive to the detecting means for decoupling said first and second signals from said gener-

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ating means when said phase relationship is outside the predetermined desired range.

2. A phase detector circuit operative in response to first and second input signals comprising means for generating a signal indicative of the phase relationship between the first and second input signals as described in claim 1 wherein said first input signal is a reference signal and said second input signal is a signal of variable frequency.

3. A phase detector circuit operative in response to first and second input signals comprising means for generating a signal indicative of the phase relationship between the first and second input signals as described in claim 2 wherein said generating means comprises a differential phase detector.

4. A phase detector circuit operative in response to first and second input signals comprising means for generating a signal indicative of the phase relationship between the first and second input signals as described in claim 3 wherein said detecting means comprises proportional phase detector means.

5. A phase detector circuit operative in response to first and second input signals comprising means for generating a signal indicative of the phase relationship between the first and second input signals as described in claim 4 wherein said proportional phase detector means comprises:

a first proportional phase detector for detecting a phase relationship between said first and second input signals that is greater in magnitude than said predetermined desired range; and

a second proportional phase detector for detecting a phase relationship between said first and second input signals that is lesser in magnitude than said predetermined desired range.

6. A phase detector for producing an error signal indicative of the phase relationship between a clock signal R and a variable frequency signal V, comprising:

a differential phase detector having first and second inputs and providing first and second output signals which constitute an error signal indicative of the phase relationship between said R signal and V signal;

a first AND gate having its output coupled to the first input of the differential phase detector and the R signal coupled to a first input thereof;

a second AND gate having its output coupled to the second input of the differential phase detector and the V signal coupled to a first input thereof;

a first DC flip flop having its output coupled to a second input of the first AND gate and having the C input thereof coupled to said V signal;

a second DC flip flop having its output coupled to a second input of the second AND gate and having the C input thereof coupled to said R signal;

a first proportional phase detector having its output coupled to the D input of the first DC flip flop and its inputs coupled to said R and V signals; and

a second proportional phase detector having its output coupled to the D input of the second D-C flip flop and its inputs coupled to said R and V signals.

7. A phase detector for producing an error signal indicative of the phase relationship between a clock signal R and a variable frequency signal V as described in claim 6 further including an integrator coupled to said first and second outputs of said differential phase detector.

* * * * *

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Klemmer et al.

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(54) **SLIP-DETECTING PHASE DETECTOR AND METHOD FOR IMPROVING PHASE-LOCK LOOP LOCK TIME**

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(58) Field of Search 327/2, 3, 5, 7, 327/8, 10, 12, 18, 22, 24, 31, 35; 324/76.77, 76.78, 76.79; 375/359, 360

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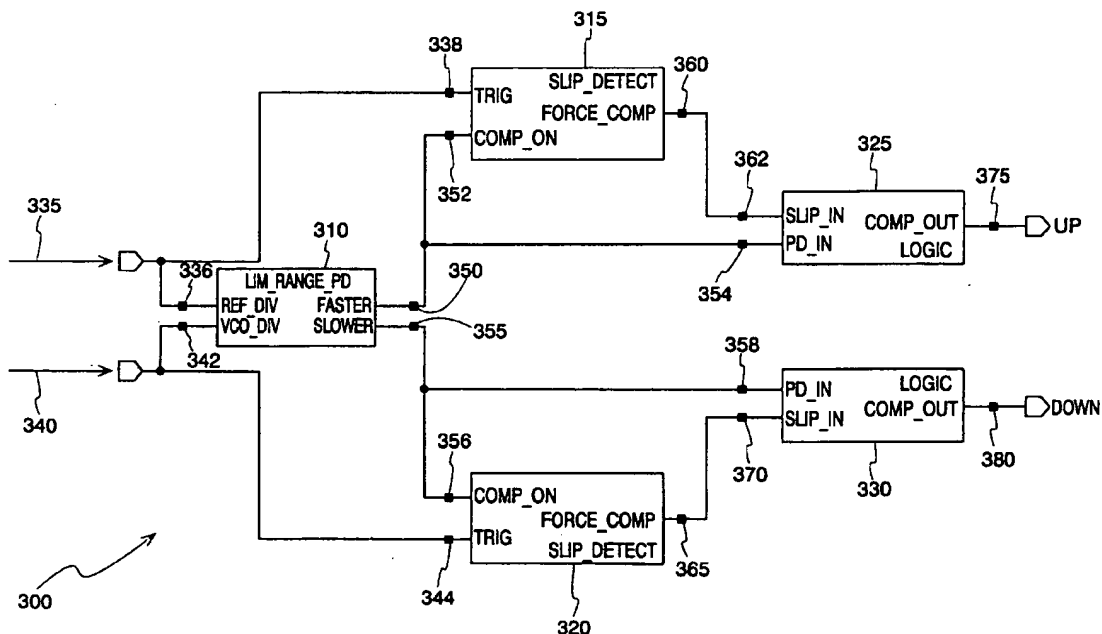
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(57)   **ABSTRACT**

An improved digital phase detector is provided for detecting and compensating for a cycle slip between a reference signal and a frequency source signal, the reference and frequency source signals each comprising pulses, each pulse defined by a leading edge and a trailing edge. The digital phase detector includes a detector circuit for detecting a cycle slip where two successive leading edges of one of the reference and frequency source signals are received before a leading edge of the other signal is received. An output circuit is operatively coupled to the detector circuit for developing a correction signal responsive to said detecting.

35 Claims, 4 Drawing Sheets

Fig. 1

Fig. 2

$$fout = \frac{N(fin)}{R}$$

Fig. 3

Compute Frequency Step
|New freq. - Old freq.| — 600

Scale into Range
$[0,2^M-1]$,
M=#bits in counter — 610

Output to Counter
Load Value — 620

Perform Channel Step — 630

640

Locked? — No

Yes

Output a Default
to Counter Load Value — 650
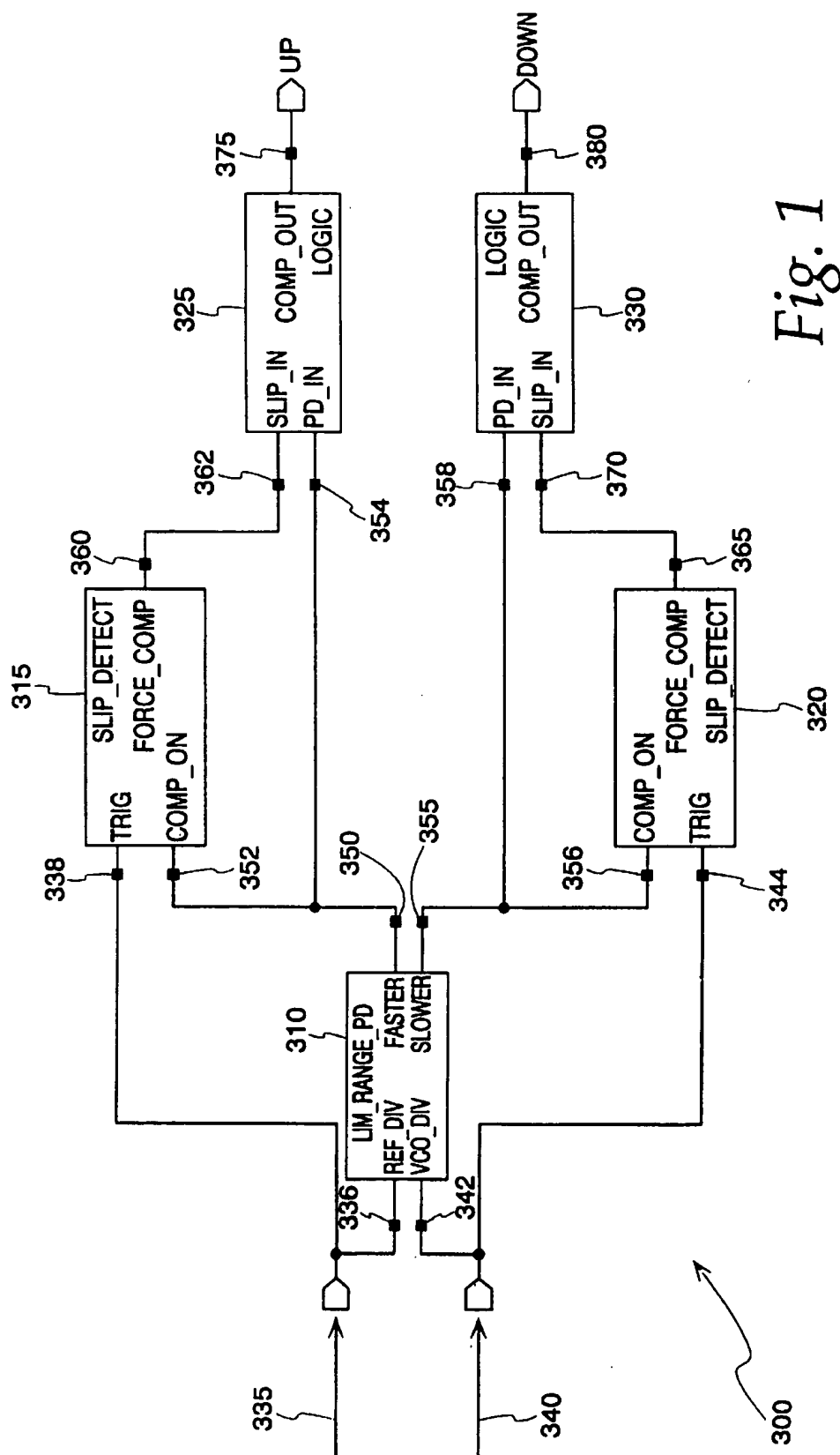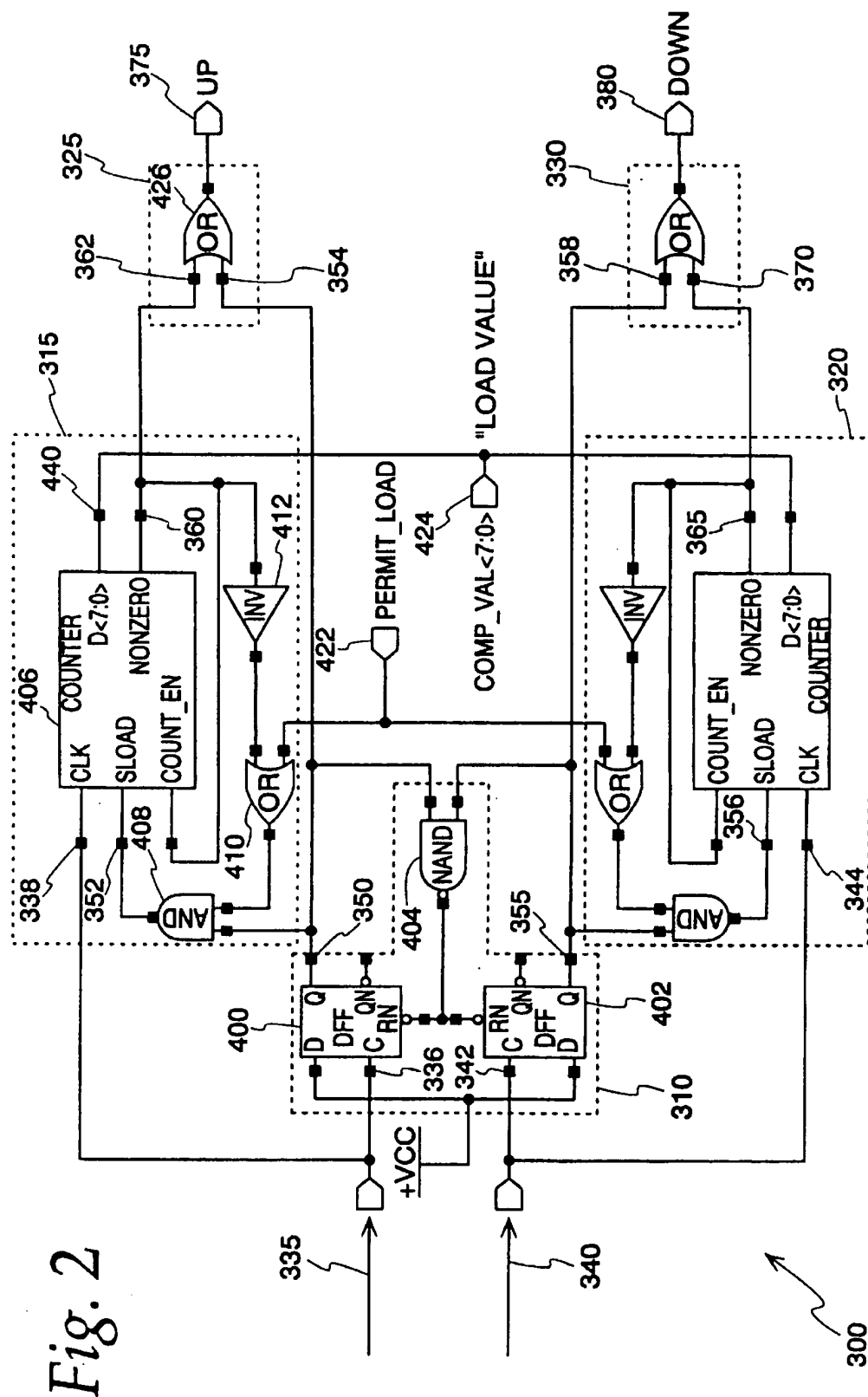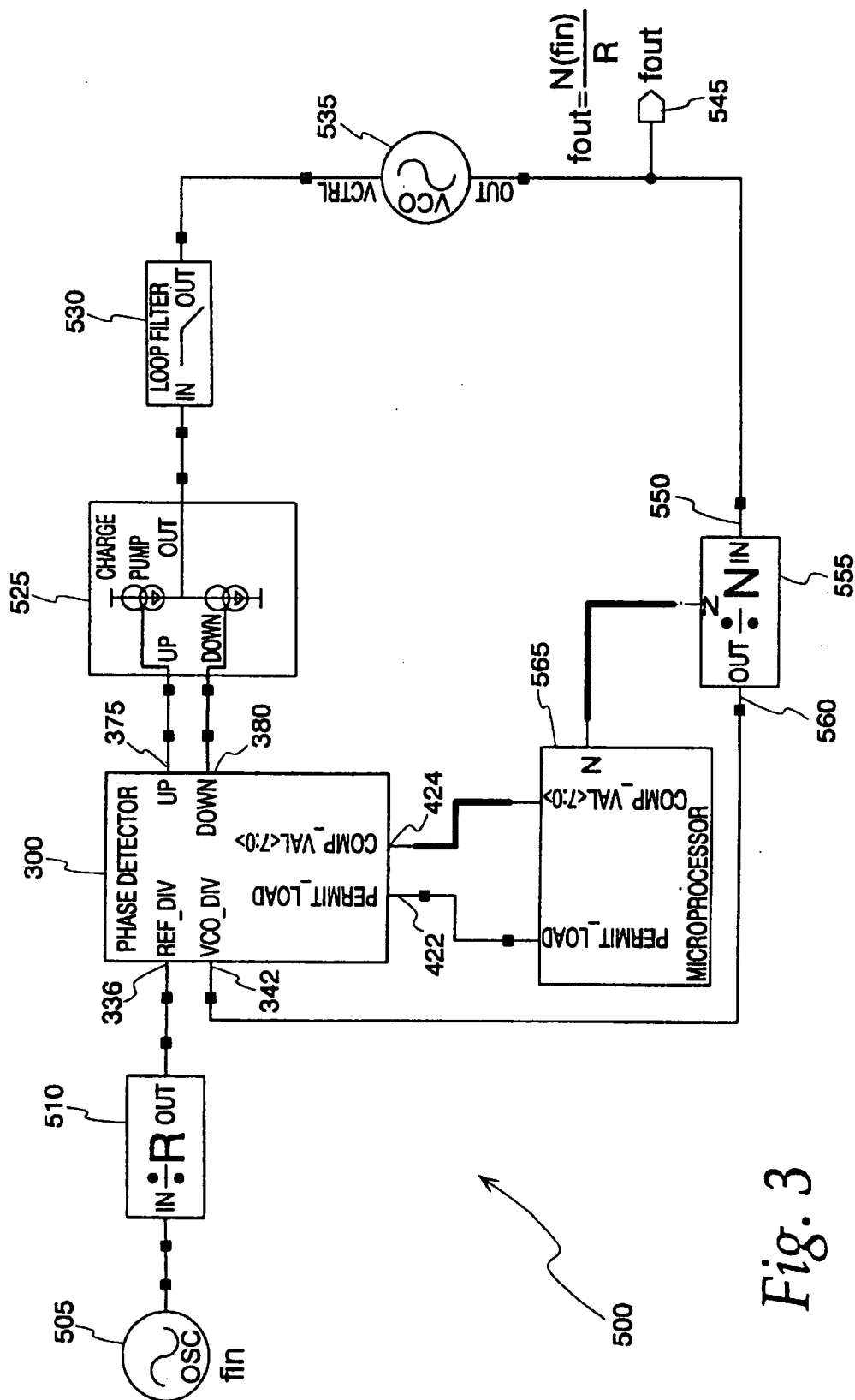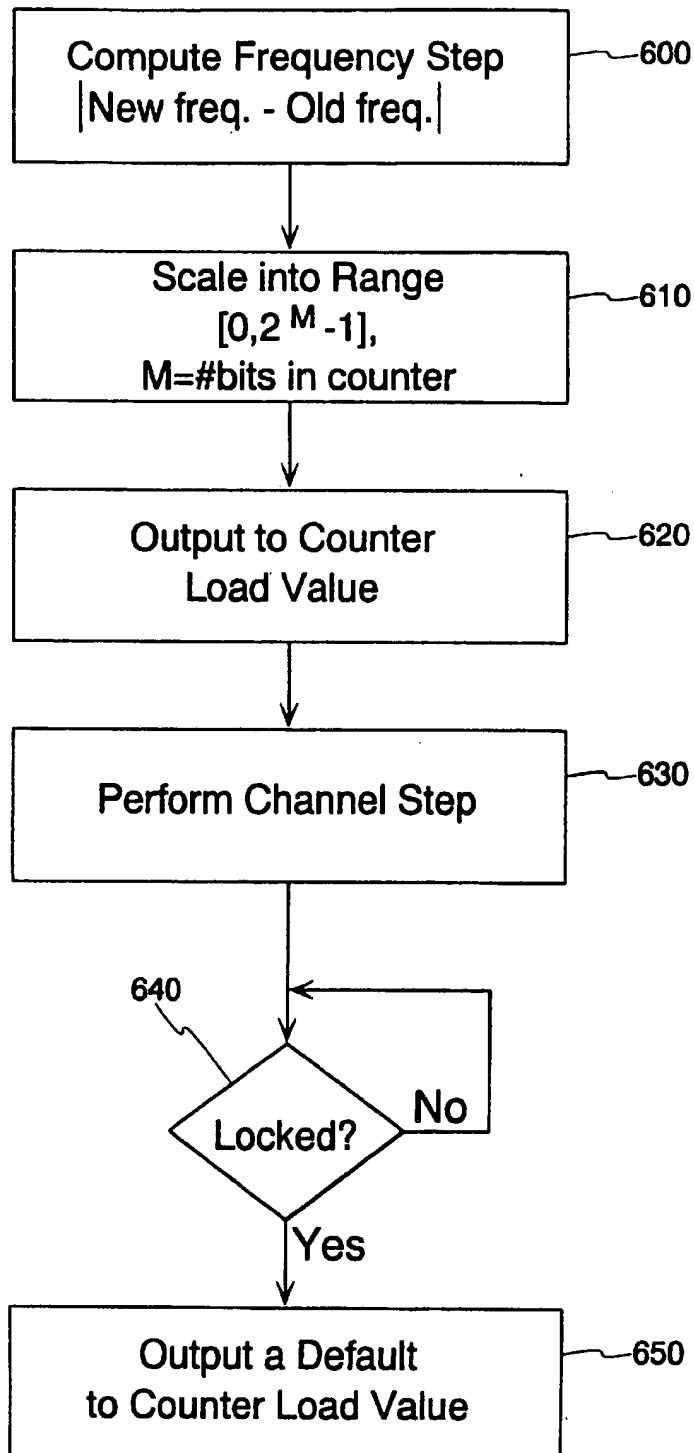
Fig. 4

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SLIP-DETECTING PHASE DETECTOR AND METHOD FOR IMPROVING PHASE-LOCK LOOP LOCK TIME

FIELD OF THE INVENTION

This invention relates to phase detectors, and more particularly, a digital phase detector with slip detection capability for reducing phase-lock loop lock time.

BACKGROUND OF THE INVENTION

A phase-locked loop (PLL), in one form, includes a phase detector, a charge pump, a loop filter, a voltage controlled oscillator (VCO) a frequency divider, and a reference frequency signal source. The PLL synthesizes a frequency source signal, for example the VCO, based on the reference frequency signal source (reference signal), for example a crystal oscillator. The phase detector keeps the frequency source and reference signals at its input equal in frequency and phase by determining a phase mismatch between the divided frequency source and reference signals, and activating the charge pump based on the amount of phase mismatch. Because of device physics, loop dynamics and system architecture, the correction cannot be made instantaneously, resulting in a finite time between the detected phase mismatch between the reference and frequency source signals and the correction of the frequency source signal. The time for the frequency source signal to achieve its intended frequency (reference frequency) is called the "lock time" of the PLL.

A digital phase detector may consist of flip-flops clocked by the edges of derivatives of the reference and frequency source signals. If one edge arrives before the other, a charge is transferred to or from a loop filter that changes the frequency of the frequency source to align the edges. The amount of charge transferred (the amount of correction) depends on the time difference between the edges of the reference and frequency source signals. However, the operating range of the digital phase detector is only -2π to 2π. An edge of the reference signal must be received for each edge of the frequency source signal for proper correction to occur. If the difference between the reference and frequency source signals is too great, two edges may appear at an input before the corresponding edge arrives at the other input. Such a situation is called a cycle slip, and leads to an improper correction, causing increased PLL lock time.

One solution to overcome the cycle slip is to extend the range of the digital phase detector. When extending the range, edges of the reference and frequency source signals are each accounted for, and as long as one input of the detector has received more edges than the other input, a correction is enabled. However, a disadvantage of simply extending the range of the phase detector is the increased overshoot in the frequency source control voltage. In voltage-limited applications, the tuning sensitivity of the voltage-controlled oscillator must be increased, resulting in higher noise, or the control voltage will reach a limit where it clips. Should the control voltage clip, the improvements in PLL lock time from using the extended range digital phase detector would be lost or even reversed.

The present invention is directed to overcoming one or more of the problems discussed above in a novel and simple manner.

SUMMARY OF THE INVENTION

In accordance with the invention, there is disclosed a digital phase detector (PD) having a slip detection circuit for

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detecting and compensating for a cycle slip, providing improved phase lock loop (PLL) lock time without clipping a control voltage of the voltage controlled oscillator.

In one aspect of the invention, an improved digital phase detector for detecting and compensating for a cycle slip between a reference signal and a frequency source signal, the reference and frequency source signals each comprising pulses, each pulse defined by a leading edge and a trailing edge, includes a detector circuit for detecting a cycle slip where two successive corresponding edges of one of the reference and frequency source signals are received before a respective corresponding edge of the other signal is received. An output circuit is operatively coupled to the detector circuit for developing a correction signal responsive to detecting a cycle slip.

In one feature of the invention, the detector circuit includes a PD for detecting a first edge of the two successive corresponding edges by detecting reception of one of a first frequency source pulse edge and a first reference signal pulse edge, and for developing a PD frequency-increase signal where the first edge is the first reference signal pulse leading edge, and developing a PD frequency-decrease signal where the first edge is the first frequency source signal pulse edge. A slip detection (SD) circuit is operatively coupled to the phase detector for receiving the reference and frequency source signals, and for detecting a second corresponding edge of the two successive corresponding edges by detecting a second corresponding reference signal edge corresponding to the first reference signal pulse edge while the frequency-increase signal is being provided, and for detecting a second corresponding frequency source pulse edge corresponding to the first frequency source pulse edge while the frequency-decrease signal is being provided. An SD frequency-increase signal is developed when the second corresponding reference signal pulse edge is detected, and an SD frequency-decrease signal is developed when the second corresponding frequency source pulse edge is detected.

In a further feature, the PD includes a pair of edge-triggered resettable flip-flops and the frequency source signal and the reference signal are clock signals for the flip-flops.

In another feature, the SD circuit includes a first counter and a second counter. The cycle slip is detected at the first counter when the second corresponding reference signal pulse edge is received at a first counter clock input while the PD frequency-increase signal is provided at a first counter comparator input, causing the first counter to load a first specified value and to provide the SD frequency-increase signal at a first counter output for the number of corresponding reference signal pulse edges equaling the first specified value. The cycle slip is detected at the second counter when the second corresponding frequency source pulse edge is received at a second counter clock input while the PD frequency-decrease signal is provided at a second counter comparator input, causing the second counter to load a second specified value and to provide the SD frequency-decrease signal at a second counter output for the number of corresponding frequency source pulse edges equaling the second specified value.

In yet a further feature, the first and second counters each have a permit load input, and including a controller coupled to the permit load inputs for allowing the first and second counters to be loaded while the respective counter is counting.

In a further feature, the first and the second counters each include a counter specified value input, and a controller

coupled to the specified value inputs provides the first and second specified values.

In a further feature, the correction signal includes at least one of an output frequency-increase signal and an output frequency-decrease signal, and the output circuit includes a first OR logic gate for developing the output frequency-increase signal responsive to the PD frequency-increase signal and the SD frequency-increase signal. The output circuit also includes a second OR logic gate for developing the output frequency-decrease signal responsive to the PD frequency-decrease signal and the SD frequency-decrease signal.

In another feature of the invention, the improved digital PD includes a controller coupled to the detector circuit and the output circuit for controlling duration of the correction signal.

In yet another feature of the invention, the two successive corresponding edges of one of the reference and frequency source signals are two successive leading edges of one of the reference and frequency source, and the respective corresponding edge of the other signal is a leading edge of the other signal.

In another aspect of the invention, an improved digital phase detector for detecting and compensating for a cycle slip between a reference signal and a frequency source signal, the reference signal and the frequency source signal each comprised of pulses defined by leading edges and trailing edges, includes a phase detector for receiving and detecting a phase difference between the reference signal and the frequency source signal, and developing a PD frequency-increase signal where a phase of the frequency source signal is lagging a phase of the reference signal, and a PD frequency-decrease signal where the phase of the frequency source signal is leading the phase of the reference signal. A slip detection circuit is operatively coupled to the phase detector, for receiving the reference signal and the frequency source signal, and for detecting slip between the reference signal and the frequency source signal, the SD circuit developing a SD frequency-increase signal where the phase detector is providing the PD frequency-increase signal and a reference signal pulse edge is detected by the SD circuit, and a SD frequency-decrease signal where the phase detector is providing the PD frequency-decrease signal and a frequency source signal pulse edge is detected by the SD circuit. An output circuit is operatively coupled to the phase detector and SD circuit for developing an output frequency-increase signal responsive to the PD and SD frequency-increase signals, and an output frequency-decrease signal responsive to the PD and SD frequency-decrease signals.

In a feature of the invention, the PD includes a pair of edge-triggered resettable flip-flops and the frequency source signal and the reference signal are clock signals for the flip-flops.

In another feature, the SD circuit includes a first counter and a second counter. Slip is detected at the first counter when a reference signal pulse edge is received at a first counter clock input while the PD frequency-increase signal is provided by the phase detector, causing the first counter to load a first specified value and provide the SD frequency-increase signal at a first counter output for the number of reference signal pulses equaling the first specified value. Slip is detected at the second counter when a frequency source signal pulse edge is received at a second counter clock input while the PD frequency-decrease signal is pro-vided by the phase detector, causing the second counter to load a second specified value and provide the SD frequency-

decrease signal at a second counter output for the number of frequency source signal pulses equaling the second specified value.

In a further feature, the first counter includes a first counter specified value input and the second counter includes a second counter specified value input, and a controller is coupled to the first and second counter specified value inputs for providing the first and second specified values respectively.

In still another feature, the first and second counters each have a permit load input, and a controller is coupled to the permit load inputs for allowing the first and second counters to be loaded while the respective counter is counting.

In another feature of the invention, the output circuit includes a first OR logic gate for developing the output frequency-increase signal responsive to the PD frequency-increase signal and the SD frequency-increase signal. The output circuit also includes a second OR logic gate for developing the output frequency-decrease signal responsive to the PD frequency-decrease signal and the SD frequency-decrease signal.

In another aspect of the invention, a method for detecting and compensating for a cycle slip between a reference signal and a frequency source signal, the reference and frequency source signals each comprising pulses, each pulse defined by a leading edge and a trailing edge, includes detecting a cycle slip where two successive corresponding edges of one of the reference and frequency source signals is received before a respective corresponding edge of the other signal. A correction signal is developed responsive to detecting a cycle slip.

In a feature of the invention, the step of detecting a cycle slip includes detecting a first edge of the two successive corresponding edges by detecting reception of one of a first frequency source pulse edge and a first reference signal pulse edge, and developing a PD frequency-increase signal where the first edge is the first reference signal pulse edge, and developing a PD frequency-decrease decrease signal where the first edge is the first frequency source pulse edge. A second corresponding edge of the two successive corre-sponding edges is detected by detecting a second corre-sponding reference signal pulse edge corresponding to the first reference signal pulse edge while the PD frequency-increase signal is being provided, and by detecting a second corresponding frequency source pulse edge corresponding to the first frequency source pulse edge while the PD frequency-decrease signal is being provided. An SD frequency-increase signal is developed when the second corresponding reference signal pulse edge is detected, and an SD frequency-decrease signal is developed when the second corresponding frequency source pulse edge is detected.

In a further feature, the step of providing the SD frequency-increase signal includes loading a first counter with a first specified value where the PD frequency-increase signal is detected at a first counter load input while the second corresponding reference signal pulse edge is detected at a first counter clock input. The SD frequency-increase signal is provided at a nonzero output of the first counter while the first counter is counting from the first specified value to zero.

In a further feature yet, the first counter is permitted to reload the first specified value while the first counter is counting from the first specified value to zero.

In a further feature, the step of loading the first counter with the first specified value includes determining the first specified value at a controller coupled to a first counter

specified value input, and providing the first specified value to the first counter specified value input.

In a further feature of the invention, the step of providing the SD frequency-decrease signal includes loading a second counter with a second specified value where the PD frequency-decrease signal is detected at a second counter load input while the second corresponding frequency source pulse edge is detected at a second counter clock input. The SD frequency-decrease signal is provided at a second counter nonzero output while the second counter is counting from the second specified value to zero.

In a further feature, the second counter is permitted to reload the second specified value while the second counter is counting from the second specified value to zero.

In a further feature, the step of loading the second counter with the second specified value includes determining the second specified value at a controller coupled to a second counter specified value input, and providing the second specified value to the second counter specified value input.

In a further feature, the step of developing a correction signal includes developing an output frequency-increase signal responsive to the PD frequency-increase signal and the SD frequency-increase signal, and developing an output frequency-decrease signal responsive to the SD frequency-decrease signal and the PD frequency-decrease signal.

In another feature of the invention, developing the correction signal includes controlling the duration of the correction signal.

In yet another feature, detecting a cycle slip where two successive corresponding edges of one of the reference and frequency source signals is received before a respective corresponding edge of the other signal includes detecting the cycle slip where two successive leading edges of one of the reference and frequency source signals is received before a leading edge of the other signal.

In another aspect of the invention, a method of detecting and compensating for a cycle slip between a reference signal and a frequency source signal in a digital phase detector, the reference signal and the frequency source signal each comprised of pulses defined by leading edges and trailing edges, includes receiving a reference signal pulse and a frequency source signal pulse. A phase difference is detected, and a PD frequency-increase signal is provided where a phase of the frequency source signal is lagging a phase of the reference signal, and a PD frequency-decrease signal is provided where the phase of the frequency source signal is leading the phase of the reference signal. An SD circuit frequency-increase signal is developed where the PD frequency-increase signal is being provided and a reference signal pulse edge is detected at an SD reference signal input, and an SD frequency-decrease signal is developed where the PD frequency-decrease signal is being provided and a frequency source signal pulse edge is detected at an SD frequency source signal input. Responsive to the PD frequency-increase signal and the SD frequency-increase signal, an output frequency-increase signal is provided, and responsive to the PD frequency-decrease signal and the SD frequency-decrease signal, an output frequency-decrease signal is provided.

In a feature of the invention, providing the SD frequency-increase signal includes loading a first counter with a first specified value where the PD frequency-increase signal is detected at a first counter load input while the reference signal pulse edge is detected at a first counter clock input, and providing the SD frequency-increase signal at a nonzero output of the first counter while the first counter is counting from the first specified value to zero.

In a further feature, the first counter is permitted to reload the first specified value while the first counter is counting from the first specified value to zero.

In a further feature, loading the first counter with the first specified value includes determining the first specified value at a controller coupled to a first counter specified value input and providing the first specified value to the first counter specified value input.

In another feature of the invention, providing the SD frequency-decrease signal includes loading a second counter with a second specified value where the PD frequency-decrease signal is detected at a second counter load input while the frequency source signal pulse edge is detected at a second counter clock input. The SD frequency-decrease signal is provided at a second counter nonzero output while the second counter is counting from the second specified value to zero.

In a further feature, the second counter is permitted to reload the second specified value while the second counter is counting from the second specified value to zero.

In a further feature, loading the second counter with the second specified value includes determining the second specified value at a controller coupled to a second counter specified value input, and providing the second specified value to the second counter specified value input.

In another feature of the invention, the output frequency-increase signal is provided at an output of a first OR gate output where at least one of the PD frequency-increase signal and the SD frequency-increase signal is being provided to the first OR gate.

In another feature, the output frequency-decrease signal is provided at an output of a second OR gate output where at least one of the PD frequency-decrease signal and the SD frequency-decrease signal is being provided to the second OR gate.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a generalized block diagram of a cycle slip detection digital phase detector in accordance with an embodiment of the invention;

FIG. 2 shows a slip detection digital phase detector circuit of FIG. 1 in greater detail;

FIG. 3 is a functional block diagram of a phase locked loop using the slip detection digital phase detector in accordance with an embodiment of the invention; and

FIG. 4 is a flow chart showing the steps to compute a load value for the slip detection digital phase detector in accordance with an embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Many of the disadvantages present with using a typical phase detector and an extended-range phase detector are overcome by using a phase detector having a slip detection circuit and an output circuit. PLL lock times are reduced compared to the typical PD. In voltage-limited applications, the tuning sensitivity of a voltage controlled oscillator (VCO) need not be changed to prevent clipping of a VCO voltage control signal. Additionally, having a controller for selecting a predetermined time period during which a correction is to be made by the slip detection circuit provides versatility, as the controller is able to tailor the phase detector with slip detection circuit to a specific situation. For example, where an operating frequency is altered by several frequency steps, a greater value for the predetermined time

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period is desired than where the operating frequency is altered by just one or two frequency steps.

Generally, the invention relates to a system and method for implementing a phase detector having a slip detection circuit and an output circuit. Thus, many disadvantages present with using a typical phase detector and an extended-range phase detector are overcome. The invention disclosed further relates to a system and method for using a controller to provide a predetermined time period during which a correction is to be made by the slip detection circuit. Such a controller provides versatility, as the controller is able to tailor the phase detector with slip detection circuit to a specific situation.

In one embodiment of the invention, a slip detection circuit is provided for detecting a cycle slip (slip condition) between a reference signal and a frequency source signal, and forcing a correction to compensate for the detected slip condition. The slip detection circuit improves PLL lock time over a typical digital phase detector (PD). The PLL lock time is reduced without a significant change in the control voltage, as compared with the extended range phase detector, thereby decreasing the chance for clipping of the control voltage signal.

FIG. 1 illustrates a cycle slip detection digital phase detector (SDPD) 300 in accordance with an embodiment of the invention. The SDPD 300 includes a phase detector (PD) 310, a first slip detection (SD) circuit 315 and a second SD 320 coupled to the phase detector 310, a first output circuit 325 coupled to the first SD circuit 315 and the PD 310, and a second output circuit 330 coupled to the second SD circuit 320 and the PD 310. A reference signal 335, for example a crystal oscillator signal, is coupled to a PD reference input 336 of the PD 310, and to a first SD trigger input 338 of the first SD 315. A frequency source signal 340, for example a VCO signal, is coupled to a PD frequency source input 342 of the PD 310, and to an second SD trigger input 344 of the second SD 320. The reference signal 335 and the frequency source signal 340 are pulse signals at the frequency of the source, formed by taking the derivative of the respective source signal. A PD frequency-increase output 350 of the PD 310 is coupled to a first SD comparator input 352 of the first SD 315. The PD frequency-increase output 350 is further coupled to a PD frequency-increase input 354 of the first output circuit 325. A PD frequency-decrease output 355 of the PD 310 is coupled to a second SD comparator input 356 of the second SD 320, and to a PD frequency-decrease input 358 of the second output circuit 330. An SD frequency-increase output 360 of the first SD 315 is coupled to an SD frequency-increase input 362 of the first output circuit 325. An SD frequency-decrease output 365 of the second SD 320 is coupled to an SD frequency-decrease input 370 of the second output circuit 330. An output circuit frequency-increase output 375 of the first output circuit 325 is coupled to a charge pump circuit (not shown). An output circuit frequency-decrease output 380 of the second output circuit 330 is also coupled to the charge pump circuit.

In operation, where the reference signal pulse of the reference signal 335 is received at the PD 310 before the frequency source signal pulse of the frequency source signal 340, a PD frequency-increase signal is generated at the PD frequency-increase output 350 for a duration of time equal to the time difference between reception of the reference signal pulse and the frequency source signal pulse at the PD 310. Where the frequency source signal pulse is received at the PD 310 before the reference signal pulse, a PD frequency-decrease signal is generated at the PD frequency-decrease output 355 for a duration of time equal to the time

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difference between reception of the frequency source signal pulse and the reference signal pulse at the PD 310.

A slip condition is detected at the first SD 315 where the PD frequency-increase signal is detected at the first SD comparator input 352 while the reference signal pulse is received at the first SD trigger input 338. However, because of a propagation delay of the PD 310, the slip condition is not detected by the first SD 315 until a second reference signal pulse of the reference signal 335 is received at the reference input 336 before the frequency source signal pulse is received at the frequency source input 342. Thus, if the second reference signal pulse is received at the reference input 336 before the frequency source signal pulse is received at the frequency source input 342, the second reference signal pulse will be received at the first SD trigger input 338 while the PD frequency-increase signal is being provided to the first SD comparator input 352, thereby causing the first SD 315 to detect the slip condition. When the slip condition is detected at the first SD 315, the SD frequency-increase output 360 provides an SD frequency-increase signal to the first output circuit 325 for a specified, or predetermined time period.

A slip condition is detected at the second SD 320 in the same fashion as at the first SD 315, except the second SD 320 looks at the PD frequency-decrease signal at the second SD comparator input 356 and the frequency source signal pulse at the second SD trigger input 344. When a slip condition is detected at the second SD 320, an SD frequency-decrease signal is provided at the SD frequency-decrease output 365 for the predetermined time period.

The first output circuit 325 provides an output circuit frequency-increase signal to the charge pump where at least one of the SD frequency-increase signal or the PD frequency-increase signal is received at the SD frequency-increase input 362 or the PD frequency-increase input 354 of the first output circuit 325. Similarly, an output circuit frequency-decrease signal is provided at the output circuit frequency-decrease output 380 where at least one of an SD frequency-decrease signal or a PD frequency-decrease signal is received at the SD frequency-decrease input 370 or a PD frequency-decrease input 358 of the second output circuit 330.

The specified, or predetermined time period is a period of time for which a correction must be provided to overcome the slip condition detected by the first SD 315 or the second SD 320. The predetermined time period may be a fixed value provided to the first SD 315 and second SD 320, or may be a variable time period provided to the first SD 315 and the second SD 320 by a controller (not shown). The method used by the controller in determining the predetermined time period is further discussed below in relation to FIG. 4.

FIG. 2 shows the slip detection digital phase detector circuit 300 in greater detail. The PD 310 includes a first edge-triggered D-type flip-flop (DFF) 400, a second edge-triggered DFF 402 and a 2-input NAND gate 404. The PD reference input 336 is a clock input of the first DFF 400, and the PD frequency source input 342 is a clock input for the second DFF 402. The "D" input for the first and second DFF 400 and 402 are coupled to +Vcc ("1"). The PD frequency-increase output 350 is the "Q" output of the first DFF 400, and the PD frequency-decrease output 355 is the "Q" output of the second DFF 402. The PD frequency-increase output 350 is coupled to one of the inputs of the 2-input NAND gate 404, and the PD frequency-decrease output 355 is coupled to the other input of the 2-input NAND gate 404. An output of the NAND gate 404 is coupled to the reset inputs of the first and second DFFs 400 and 402.

The first SD **315** includes an edge-triggered counter **406**, here an 8-bit counter sufficient for counting down from **255**, a first 2-input AND gate **408**, a first 2-input OR gate **410**, and a first inverter gate **412**. The first SD trigger input **338** is a clock input of the counter **406**, the first SD comparator input **352** is an s-load input of the counter **406**, and the SD frequency-increase output **360** is the nonzero output of the counter **406**, which generates a logic "1" while the counter **406** is counting. The reference signal **335** is coupled to both the PD reference input **336** of the first DFF **400** and to the first SD trigger input **338** of the counter **406**. The SD frequency-increase output **360** is coupled to a count enable input of the counter **406**, which enables the counter **406** to count while a logical "1" is provided, and to an input of the first inverter gate **412**. An output of the inverter gate **412** is coupled to one of the inputs of the 2-input OR gate **410**. An output of the OR gate **410** is coupled to one of the inputs of the 2-input AND gate **408**. The other input of the 2-input AND gate **408** is coupled to the PD frequency-increase output **350** of the first DFF **400**. The output of the AND gate **408** is coupled to the first SD comparator input **352**.

A second input of the 2-input OR gate **410** is coupled to a permit-load terminal **422**, which may be coupled to a controller (not shown). A counter value input **440** of the counter **406** is coupled to a load value terminal **424**, which may also be coupled to the controller. The load value terminal **424** provides a load value to the counter value input **440**, which governs the predetermined time period for which a correction will be provided when a slip condition is detected. Although shown as a single signal line, the connection from the counter value input **440** to the load value terminal **424** may be a plurality of lines sufficient for providing a binary load value for the counter **406**. For example, where the counter **406** is an 8-bit counter for counting down from **255**, eight signal lines would be provided coupling the load value terminal **424** to the counter value input **440**.

The second SD **320** is constructed in an identical fashion and will not be described in detail.

The first output circuit **325** includes an output circuit 2-input OR gate **426**, where the SD input **362** is one input of the OR gate **426**, and the PD input **354** is the other input of the OR gate **426**. The SD frequency-increase output **360** is coupled to the SD input **362** of the output circuit OR gate **426**, and the PD frequency-increase output **350** is coupled to the PD input **354** of the output circuit OR gate **426**. The output circuit frequency-increase output **375** is an output of the OR gate **426**, and is coupled to the charge pump circuit (not shown). The second output circuit **330** is constructed in an identical fashion and will not be discussed in detail.

In the preferred embodiment, the first and second DFFs **400** and **402** and the counter **406** are leading edge-triggered, where the DFFs and counter are only triggered on the rising edge of a signal.

When waiting for a slip condition to occur, the SD frequency-increase output **360** is at logical "0", causing a "1" at the output of the inverter gate **412**, and in turn providing a logical "1" to one of the inputs of the two-input AND gate **408** via the OR gate **410**. At this time, the SDPD **300** acts like the typical phase detector circuit as is known in the art. The slip condition is detected by the first SD **315** when two successive corresponding edges of the reference signal **335**, for example leading edges of two successive reference signal pulses of the reference signal **335**, are received before a respective corresponding edge of the other signal, for example a leading edge of a frequency source

signal pulse of the frequency source signal **340**. When the leading edge of the second reference signal pulse is received before the leading edge of the frequency source pulse, the leading edge of the second reference signal pulse is received at the first SD trigger input **338** while a logical "1" is provided at the first SD comparator input **352**. Thus, when the PD **310** is providing a correction at the PD frequency-increase output **350** while a reference signal pulse leading edge is received at the first SD trigger input **338**, the counter **406** loads the load value provided at the load value input **424**, and begins counting from the load value to zero. The SD frequency-increase output becomes logical "1", forcing a correction at the first output circuit **325** for the number of reference signal pulses received at the first SD trigger input **338** equaling the load value.

Because of the propagation delay of the first DFF **400**, a leading edge of a first reference signal pulse provided to the first SD trigger input **338** is not present when the PD frequency-increase signal is provided at the PD frequency-increase output **350**, preventing the counter **406** from loading the load value provided at the load value terminal **424**. However, where the leading edge of the second reference signal pulse is received at the SDPD **300** before the frequency source signal pulse is received at the frequency source input **342**, the leading edge of the second reference signal pulse is present at the first SD trigger input **338** while the first AND gate **408** is providing a "1" to the first SD comparator input **352**, causing the counter **406** to load the load value and begin counting, thereby forcing the correction.

When the counter **406** is counting, the SD frequency-increase output **360** becomes a "1", providing a "1" to the count enable input of the counter **406**, enabling the counter **406** to count down from the load value to zero, clocked by subsequent pulses of the reference signal **335**. Further, a "1" present at the SD frequency-increase output **360** provides a zero to the first input of the first OR gate **410** via the inverter **412**, thereby providing a zero to one of the inputs of the 2-input AND gate **408**, preventing the counter **406** from re-loading the load value from the load value terminal **424** until the counter **406** has completed counting from the load value to zero. While the counter **406** is counting from the load value to zero, the SD frequency-increase output **360** causes the first output circuit **325** to provide the output circuit frequency-increase signal from the output circuit frequency-increase output **375** to the charge pump.

The second SD **320** and second output circuit **330** operate in an identical fashion and will not be discussed.

In a further embodiment, the permit load terminal **422** may provide a "1" to the first OR gate **410**, thereby permitting the counter **406** to be reloaded when additional slip conditions are detected at the first SD **315** while a correction is being made. In this embodiment, the permit load terminal **422** may be coupled to a controller (not shown) which provides the value to the permit load terminal **422** based on channel characteristics of the received signal. Alternatively, the permit load terminal may be hardwired to provide a logical "1" or "0".

The load value terminal **424** may be hardwired with a specific load value. Alternatively, the load value terminal **424** may be coupled to the controller, where the controller provides the value to be loaded to the counter **406**, further discussed in relation to FIG. **4**. In a preferred embodiment, the load value terminal provides a value of **31** to the counter **406**, thereby causing a correction lasting **31** reference signal pulses when slip is detected by the first SD **315**.

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FIG. 3 is a functional block diagram of a PLL 500 using the SDPD 300 in accordance with an embodiment of the invention. In this case, the PLL 500 may be used in a cellular telephone, where the output of the PLL is provided to a mixer in the cellular telephone for mixing a received signal to an intermediate or a baseband frequency. An oscillator 505 for providing a reference signal is coupled to a frequency divider 510, which divides the reference signal by a factor "R", providing the reference signal 335 to the PD reference input 336 of the PD 300. A charge pump 525 is coupled to the output circuit frequency-increase output 375 and the output circuit frequency-decrease output 380. The charge pump 525 is coupled to a loop filter 530 for filtering an output signal from the charge pump 525, for use as a control signal for a VCO 535. An output of the VCO 535 is coupled to an input 550 of a frequency source frequency divider 555, which divides a frequency provided at the input 550 by a value of "N". An output of the frequency source frequency divider 555 is coupled to the frequency source input 342. A controller 565 in the form of a programmed microprocessor is coupled to the permit load terminal 422 and the load value terminal 424, and may provide the load value and/or a permit load signal to the SDPD 300. The controller 540 is further coupled to the output frequency divider 555, providing the value "N" at which the frequency source frequency divider 555 is to operate, as is known by one skilled in the art. The output of the VCO 535 is further coupled to a PLL output 545, which provides a frequency output value of N(fin)/R to a mixer (not shown) for mixing a signal received at the cellular telephone to an intermediate or a baseband frequency, where fin is the frequency provided by the oscillator 505.

Having the slip detection digital phase detector allows a slip condition to be detected, and a correction to be forced for the predetermined time period to compensate for the slip condition. In this way, the PLL lock time is improved over that of a typical digital phase detector without a significant change in the control voltage, as compared with the extended range phase detector, thereby decreasing the chance for clipping of the control voltage.

In another embodiment of the invention, a controller is provided for selecting the predetermined time period during which a correction is to be made by the slip detection circuit. The predetermined time period is governed by the load value determined by the controller. Having the controller which provides a variable load value to the SDPD 300 provides versatility, as the controller is able to tailor the phase detector with slip detection circuit to a specific situation. For example, when the SDPD 300 is used in a cellular telephone, and it is necessary to change the operating frequency of the cellular telephone, alteration of the operating frequency by a small number of frequency channels may require a smaller load value than alteration of the operating frequency of the cellular telephone by several frequency channels.

FIG. 4 is a flow chart showing operation of the controller to compute a load value for the slip detection digital phase detector circuit, in accordance with an embodiment of the invention. At step 600, the frequency step is computed by taking the absolute value of the difference between a new, or target operating frequency and an old, or current operating frequency. The frequency step is scaled into the counter range by determining the load value to be provided to the counter 406 via the load value input 424, as shown in step 610. Step 610 may be accomplished using a table indexed by the frequency step, where a load value is retrieved from the table based on the frequency step determined in step 600. The load values stored in the table may be determined

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experimentally for the specific system, and the table may include a single load value, or a plurality of load values. Step 610 may also be accomplished using a formula present in the controller, where the load value is a function of the frequency step, and takes into account characteristics of the charge pump, the loop filter and voltage controlled oscillator. The controller then outputs the load value to the counter value input 440 of the counter 406 as shown in step 620. The channel step is then performed, as shown in step 630, where a device in which the SDPD 300 is disposed changes the operating frequency to the target frequency. In step 640, it is determined whether the PLL has locked. A lock detection circuit, known in the art, indicates to the controller whether the PLL has locked. If the PLL has locked, a default load value is provided to the counter of the SDPD 300, shown in step 650, where the default load value is typically much less than the load value determined in step 610. However, if the PLL has not locked, the method returns to step 640, where the SDPD 300 provides corrections until the PLL is determined to have locked.

In an alternate embodiment, the load value provided to the counters 406 and 414 could be changed during the locking transient, for example by halving the load value every 50 us. This would reduce the amount of slip compensation as the frequencies at the phase detector inputs become closer, reducing the chance for voltage overshoot. Further, the permit load terminal 422 could initially be active and switched inactive during the locking transient, preventing the counters from re-loading until the correction made by the first SD 315 or second SD 320 has been completed.

Thus, having the controller which provides a variable load value to the SDPD 300 provides versatility, as the controller is able to tailor the phase detector with slip detection circuit based on the specific operating conditions, for example the change in the frequency step.

One skilled in the art would realize that although the slip detection digital phase detector has been explained in the context of a cellular telephone, the slip detection digital phase detector may be used in any context a digital phase detector is needed, for example, RADAR and computer disk drives.

One skilled in the art would further realize that although the first and second DFFs 400 and 402, and the counter 406 have been described as leading edge-triggered circuits, the first and second DFFs and counter may alternatively be trailing edge-triggered circuits, where the first and second DFFs and counter are triggered by a trailing edge of the signal.

A slip detection digital phase detector is provided having the slip detection circuit which allows a slip condition to be detected, and permits a correction to be forced for the predetermined time period to compensate for the slip condition. PLL lock time is improved over that of a typical digital phase detector (DPD) without a significant change in the control voltage, as compared with the extended range phase detector, thereby decreasing the chance for clipping of the control voltage. Further provided is the controller which provides the predetermined time period for a correction to the SDPD 300. The controller provides versatility, as the predetermined time period may be tailored based on the specific operating conditions, for example the change in the operating frequency.

While particular embodiments of the invention have been described and illustrated, it should be understood that the invention is not limited thereto since modifications may be made by persons skilled in the art. The present application

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contemplates any and all modifications that fall within the spirit and scope of the underlying invention disclosed and claimed herein.

We claim:

1. An improved digital phase detector (PD) for detecting and compensating for a cycle slip between a reference signal and a frequency source signal, the reference and frequency source signals each comprising pulses, each pulse defined by a leading edge and a trailing edge, the digital PD comprising:

    a detector circuit for detecting a cycle slip where two successive corresponding edges of one of the reference and frequency source signals are received before a respective corresponding edge of the other signal is received; and

    an output circuit operatively coupled to the detector circuit for developing a correction signal responsive to detecting a cycle slip.

2. The improved digital phase detector of claim 1 wherein the detector circuit includes:

    a PD for detecting a first edge of the two successive corresponding edges by detecting reception of one of a first frequency source pulse edge and a first reference signal pulse edge, and for developing a PD frequency-increase signal where the first edge is the first reference signal pulse, and developing a PD frequency-decrease signal where the first edge is the first frequency source signal pulse edge; and

    a slip detection (SD) circuit operatively coupled to the phase detector for receiving the reference and frequency source signals, and for detecting a second corresponding edge of the two successive corresponding edges by detecting a second corresponding reference signal pulse edge corresponding to the first reference signal pulse edge while the frequency-increase signal is being provided, and by detecting a second corresponding frequency source pulse edge corresponding to the first frequency source pulse edge while the frequency-decrease signal is being provided;

    wherein an SD frequency-increase signal is developed when the second corresponding reference signal pulse edge is detected, and an SD frequency-decrease signal is developed when the second corresponding frequency source pulse edge is detected.

3. The improved digital phase detector of claim 2 wherein the PD includes a pair of edge-triggered resettable flip-flops and the frequency source signal and the reference signal are clock signals for the flip-flops.

4. The improved digital phase detector of claim 2 wherein the SD circuit includes a first counter and a second counter,

    wherein the cycle slip is detected at the first counter when the second corresponding reference signal pulse edge is received at a first counter clock input while the PD frequency-increase signal is provided at a first counter comparator input, causing the first counter to load a first specified value and to provide the SD frequency-increase signal at a first counter output for the number of corresponding reference signal pulse edges equaling the first specified value, and

    the cycle slip is detected at the second counter when the second corresponding frequency source signal pulse edge is received at a second counter clock input while the PD frequency-decrease signal is provided at a second counter comparator input, causing the second counter to load a second specified value and to provide the SD frequency-decrease signal at a second counter

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output for the number of corresponding frequency source pulse edges equaling the second specified value.

5. The improved digital phase detector of claim 4, wherein the first and second counters each have a permit load input, and including a controller coupled to the permit load inputs for allowing the first and second counters to be loaded while the respective counter is counting.

6. The improved digital PD of claim 4 wherein the first and the second counters each include a counter specified value input, and further including a controller coupled to the specified value inputs for providing the first and second specified values.

7. The improved digital PD of claim 2 wherein the correction signal includes at least one of an output frequency-increase signal and an output frequency-decrease signal, and the output circuit includes:

    a first OR logic gate for developing the output frequency-increase signal responsive to the PD frequency-increase signal and the SD frequency-increase signal; and

    a second OR logic gate for developing the output frequency-decrease signal responsive to the PD frequency-decrease signal and the SD frequency-decrease signal.

8. The improved digital PD of claim 1 including a controller coupled to the detector circuit and the output circuit for controlling duration of the correction signal.

9. The improved digital PD of claim 1 wherein the two successive corresponding edges of one of the reference and frequency source signals are two successive leading edges of one of the reference and frequency source signals, and the respective corresponding edge of the other signal is a leading edge of the other signal.

10. An improved digital phase detector for detecting and compensating for a cycle slip between a reference signal and a frequency source signal, the reference signal and the frequency source signal each comprised of pulses defined by leading edges and trailing edges, including:

    a phase detector (PD) for receiving and detecting a phase difference between the reference signal and the frequency source signal, and developing a PD frequency-increase signal where a phase of the frequency source signal is lagging a phase of the reference signal, and a PD frequency-decrease signal where the phase of the frequency source signal is leading the phase of the reference signal;

    a slip detection (SD) circuit operatively coupled to the phase detector, for receiving the reference signal and the frequency source signal, and for detecting slip between the reference signal and the frequency source signal, the SD circuit developing a SD frequency-increase signal where the phase detector is providing the PD frequency-increase signal and a reference signal pulse edge is detected by the SD circuit, and a SD frequency-decrease signal where the phase detector is providing the PD frequency-decrease signal and a frequency source signal pulse edge is detected by the SD circuit; and

    an output circuit operatively coupled to the phase detector and SD circuit for developing an output frequency-increase signal responsive to the PD and SD frequency-increase signals, and an output frequency-decrease signal responsive to the PD and SD frequency-decrease signals.

11. The improved digital phase detector of claim 10 wherein the phase detector includes a pair of edge-triggered

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resettable flip-flops and the frequency source signal and the reference signal are clock signals for the flip-flops.

12. The improved digital phase detector of claim 10 wherein the SD circuit includes a first counter and a second counter,

wherein slip is detected at the first counter when a reference signal pulse edge is received at a first counter clock input while the PD frequency-increase signal is provided by the phase detector, causing the first counter to load a first specified value and provide the SD frequency-increase signal at a first counter output for the number of reference signal pulses equaling the first specified value, and

slip is detected at the second counter when a frequency source signal pulse edge is received at a second counter clock input while the PD frequency-decrease signal is provided by the phase detector, causing the second counter to load a second specified value and provide the SD frequency-decrease signal at a second counter output for the number of frequency source signal pulses equaling the second specified value.

13. The improved digital phase detector of claim 12 wherein the first counter includes a first counter specified value input and the second counter includes a second counter specified value input, and further including a controller coupled to the first and second counter specified value inputs for providing the first and second specified values respectively.

14. The improved digital phase detector of claim 12 wherein the first and second counters each have a permit load input, and including a controller coupled to the permit load inputs for allowing the first and second counters to be loaded while the respective counter is counting.

15. The improved digital phase detector of claim 10 wherein the output circuit includes:

a first OR logic gate for developing the output frequency-increase signal responsive to the PD frequency-increase signal and the SD frequency-increase signal; and

a second OR logic gate for developing the output frequency-decrease signal responsive to the PD frequency-decrease signal and the SD frequency-decrease signal.

16. A method for detecting and compensating for a cycle slip between a reference signal and a frequency source signal, the reference and frequency source signals each comprising pulses, each pulse defined by a leading edge and a trailing edge, the method comprising:

detecting a cycle slip where two successive corresponding edges of one of the reference and frequency source signals are received before a respective corresponding edge of the other signal; and

developing a correction signal responsive to detecting a cycle slip.

17. The method of claim 16 wherein the step of detecting a cycle slip includes:

detecting a first edge of the two successive corresponding edges by detecting reception of one of a first frequency source pulse edge and a first reference signal pulse edge, and developing a PD frequency-increase signal where the first edge is the first reference signal pulse edge, and developing a PD frequency-decrease signal where the first edge is the first frequency source pulse edge; and

detecting a second corresponding edge of the two successive corresponding edges by detecting a second

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corresponding reference signal pulse edge corresponding to the first reference signal pulse edge while the PD frequency-increase signal is being provided, and by detecting a second corresponding frequency source pulse edge corresponding to the first frequency source pulse edge while the PD frequency-decrease signal is being provided, wherein an SD frequency-increase signal is developed when the second corresponding reference signal pulse edge is detected, and an SD frequency-decrease signal is developed when the second corresponding frequency source pulse edge is detected.

18. The method of claim 17 wherein the step of providing the SD frequency-increase signal includes:

loading a first counter with a first specified value where the PD frequency-increase signal is detected at a first counter load input while the second corresponding reference signal pulse edge is detected at a first counter clock input; and

providing the SD frequency-increase signal at a non zero output of the first counter while the first counter is counting from the first specified value to zero.

19. The method of claim 18 including the step of permitting the first counter to reload the first specified value while the first counter is counting from the first specified value to zero.

20. The method of claim 18 wherein the step of loading the first counter with the first specified value includes:

determining the first specified value at a controller coupled to a first counter specified value input; and

providing the first specified value to the first counter specified value input.

21. The method of claim 17 wherein the step of providing the SD frequency-decrease signal includes:

loading a second counter with a second specified value where the PD frequency-decrease signal is detected at a second counter load input while the second corresponding frequency source pulse edge is detected at a second counter clock input; and

providing the SD frequency-decrease signal at a second counter nonzero output while the second counter is counting from the second specified value to zero.

22. The method of claim 21 including the step of permitting the second counter to reload the second specified value while the second counter is counting from the second specified value to zero.

23. The method of claim 21 wherein the step of loading the second counter with the second specified value includes:

determining the second specified value at a controller coupled to a second counter specified value input; and

providing the second specified value to the second counter specified value input.

24. The method of claim 17 wherein the step of developing a correction signal includes:

developing an output frequency-increase signal responsive to the PD frequency-increase signal and the SD frequency-increase signal; and

developing an output frequency-decrease signal responsive to the SD frequency-decrease signal and the PD frequency-decrease signal.

25. The method of claim 16 wherein the step of developing the correction signal includes controlling the duration of the correction signal.

26. The method of claim 16 wherein the step of detecting a cycle slip where two successive corresponding edges of

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one of the reference and frequency source signals is received before a respective corresponding edge of the other signal includes detecting the cycle slip where two successive leading edges of one of the reference and frequency source signals is received before a leading edge of the other signal.

27. A method of detecting and compensating for a cycle slip between a reference signal and a frequency source signal in a digital phase detector, the reference signal and the frequency source signal each comprised of pulses defined by leading edges and trailing edges, comprising:

receiving a reference signal pulse and a frequency source signal pulse;

detecting a phase difference and providing a phase detector (PD) frequency-increase signal where a phase of the frequency source signal is lagging a phase of the reference signal, and providing a PD frequency-decrease signal where the phase of the frequency source signal is leading the phase of the reference signal;

providing a slip detector (SD) circuit frequency-increase signal where the PD frequency-increase signal is being provided and a reference signal pulse edge is detected at an SD reference signal input, and providing an SD frequency-decrease signal where the PD frequency-decrease signal is being provided and a frequency source signal pulse edge is detected at an SD frequency source signal input;

responsive to the PD frequency-increase signal and the SD frequency-increase signal, providing an output frequency-increase signal; and

responsive to the PD frequency-decrease signal and the SD frequency-decrease signal, providing an output frequency-decrease signal.

28. The method of claim 27 wherein the step of providing the SD frequency-increase signal includes:

loading a first counter with a first specified value where the PD frequency-increase signal is detected at a first counter load input while the reference signal pulse edge is detected at a first counter clock input; and

providing the SD frequency-increase signal at a nonzero output of the first counter while the first counter is counting from the first specified value to zero.

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29. The method of claim 28 including the step of permitting the first counter to reload the first specified value while the first counter is counting from the first specified value to zero.

30. The method of claim 28 wherein the step of loading the first counter with the first specified value includes:

determining the first specified value at a controller coupled to a first counter specified value input; and

providing the first specified value to the first counter specified value input.

31. The method of claim 27 wherein the step of providing the SD frequency-decrease signal includes:

loading a second counter with a second specified value where the PD frequency-decrease signal is detected at a second counter load input while the frequency source signal pulse edge is detected at a second counter clock input; and

providing the SD frequency-decrease signal at a second counter nonzero output while the second counter is counting from the second specified value to zero.

32. The method of claim 31 including the step of permitting the second counter to reload the second specified value while the second counter is counting from the second specified value to zero.

33. The method of claim 31 wherein the step of loading the second counter with the second specified value includes:

determining the second specified value at a controller coupled to a second counter specified value input; and

providing the second specified value to the second counter specified value input.

34. The method of claim 27 including providing the output frequency-increase signal at an output of a first OR gate output where at least one of the PD frequency-increase signal and the SD frequency-increase signal is being provided to the first OR gate.

35. The method of claim 27 including providing the output frequency-decrease signal at an output of a second OR gate output where at least one of the PD frequency-decrease signal and the SD frequency-decrease signal is being provided to the second OR gate.

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